OUTLINE

The RP901xxxx is a CMOS-based current mode PWM control synchronous step-down DC/DC converter with a
voltage detector (VD) and an LDO regulator (VR).

Each of Step-down DC/DC converters is composed of an oscillator, a voltage reference unit, an error amplifier, a
switching control circuit, a soft-start circuit, a protection circuit, a UVLO circuit, a switching transistor. Due to the
switching elements are built in and synchronous control, a high efficiency step-down DC/DC converter can be
made with an inductor and capacitors. To realize high efficiency at light load, automatic PWM/VFM alternative
mode can be selected other than the PWM fixed control mode.

As protection circuits, a current limit circuit which limits Lx peak current cycle by cycle and a hiccup mode
protection circuit which works if the load current over the limit continues for a certain time\(^1\) are built in. The output
voltage can be preset with 0.05V step in the factory due to the built-in feed back resistance, and the tolerance is
±2%. Since the package is DFN (PLP) 2527-10, high density mounting on board is possible.

Built-in LDO regulator (VR) is composed of a voltage reference unit, a voltage detecting resistor-network, an
error amplifier, a short current limit circuit, and a driver transistor. After the soft-start time of the DC/DC converter
is over and a specified delay time, LDO starts up. The sequence function is fixed internally\(^2\).

Built-in voltage detector (VD) supervises the input voltage or the output of the VR (The reset function works for
UVLO and over-current of the DC/DC converter). The option is preset in the factory. The output type is N-channel
open drain. The released delay time is built-in, typ.50ms.

If the junction temperature of the IC is over the limit, the system is reset by the built-in thermal shut-down circuit.

\(^1\) A version: As soon as the load current is over the limit, the system restarts by the protection.

\(^2\) C, D versions: No sequence function

FEATURES

- Input Voltage Range .................................................. 4.5V to 5.5V
- Supply Current ......................................................... Typ. 460µA (at PWM mode) Typ. 170µA (at light load applied to B, C, D versions)

Step-down DC/DC Converter

- Output Voltage Range ............................................... 1.2V to 1.8V, preset is possible by user’s request
- Output Voltage Tolerance ........................................... ±2%
- Oscillator Frequency ................................................. Typ. 1.2MHz
- Built-in driver ON resistance ...................................... Typ. P-channel 0.25Ω, N-channel 0.25Ω (at VIN=5V)
- Soft-start function ..................................................... Typ. 1ms
- Lx peak current limit function ..................................... Typ. 1.4A (D version: 1.5A)
- Output Current ........................................................ Min. 800mA (D version: 900mA)
- Protection Delay Time ................................................. Typ. 0.1ms (applied to B, C, D versions)
- UVLO function .......................................................... Typ. 3.5V
- Chip enable function ................................................ "H" active
LDO Regulator
- Output Voltage Range: 2.5V to 3.3V, preset is possible by user's request
- Output Voltage Tolerance: ±1.0%
- Output Current: Min. 600mA
- Start-up delay time: Typ. 2ms (applied to A, B versions)
- Auto-Discharge function at turning off: Discharge resistance Typ. 50Ω (at VIN=5V)

VD
- Voltage Detector Threshold Range: 2.0V to 3.0V, preset is possible by user's request
  (A version: VR output voltage is supervised), 3.0V to 5.0V, preset is possible by user's request
  (B, C, D versions: Input voltage is supervised)
- Released Delay Time: Typ. 50ms
- Thermal shutdown circuit: Detecting Temperature: Typ. 165°C, Released temperature: Typ. 110°C
- Package: DFN(PLP)2527-10
- External Components: C_{in}=10.0\mu F, C_{OUT1}=10.0\mu F, L=4.7\mu H (DC/DC), C_{OUT2}=2.2\mu F (VR)

APPLICATION
- Optical Disk Equipment
BLOCK DIAGRAMS

A version

B/C/D version
SELECTION GUIDE

In the RP901 series, the output voltage combination and function can be designated. The selection can be made by the alphanumeric serial number as the next example.

<table>
<thead>
<tr>
<th>Product Code</th>
<th>Package</th>
<th>Units/1 reel</th>
<th>Pb free</th>
<th>Halogen free</th>
</tr>
</thead>
<tbody>
<tr>
<td>RP901Kxxx*-TR</td>
<td>DFN(PLP)2527-10</td>
<td>5,000pcs</td>
<td>Yes</td>
<td>Yes</td>
</tr>
</tbody>
</table>

xxx: Serial number to describe the voltage combination of DC/DC converter, voltage regulator, and voltage detector.

*: Function version

A version: DC/DC control type is PWM-fixed, without protection delay time, output current Min. 800mA, VR has start-up delay time to make a sequence. VD supervises the output of VR (Reset is output at UVLO and over current of DC/DC)

B version: DC/DC control type is PWM/VFM automatic mode shift, with protection delay time, output current Min. 800mA, VR has start-up delay time to make a sequence. VD supervises the input voltage.

C version: DC/DC control type is PWM/VFM automatic mode shift, with protection delay time, output current Min. 800mA, VR: without delay time to make a sequence, VD supervises the input voltage.

D version: DC/DC control type is PWM/VFM automatic mode shift, with protection delay time, output current Min. 900mA, VR: without delay time to make a sequence, VD supervises the input voltage.

PIN CONFIGURATION

DFN(PLP)2527-10

Mark Side

Bottom Side

Steam via
## PIN DESCRIPTIONS

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>CE</td>
<td>Chip Enable Pin (&quot;H&quot; active)</td>
</tr>
<tr>
<td>2</td>
<td>V_{DOUT}</td>
<td>VD Output Pin (N-channel open drain output)</td>
</tr>
<tr>
<td>3</td>
<td>AGND</td>
<td>Analog Ground Pin</td>
</tr>
<tr>
<td>4</td>
<td>PGND</td>
<td>Power Ground Pin</td>
</tr>
<tr>
<td>5</td>
<td>L_{X}</td>
<td>DC/DC Switching Pin</td>
</tr>
<tr>
<td>6</td>
<td>PVDD</td>
<td>Power Supply Input Pin</td>
</tr>
<tr>
<td>7</td>
<td>NC</td>
<td>No connection</td>
</tr>
<tr>
<td>8</td>
<td>V_{OUT1}</td>
<td>DC/DC Output Pin</td>
</tr>
<tr>
<td>9</td>
<td>AVDD</td>
<td>Analog Power Supply Input Pin</td>
</tr>
<tr>
<td>10</td>
<td>V_{OUT2}</td>
<td>VR Output Pin</td>
</tr>
</tbody>
</table>

The backside of the package tab is connected to the substrate of the IC (GND). Connect to GND pin (Recommendation), or solder the tab and left open electrically. Make short 3pin and 4pin, and make short 6pin and 9pin.

## ABSOLUTE MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Item</th>
<th>Rating</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_{IN}</td>
<td>PVDD Pin Voltage</td>
<td>6.5 V</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>AVDD Pin Voltage</td>
<td></td>
<td></td>
</tr>
<tr>
<td>V_{CE}</td>
<td>CE Pin Voltage</td>
<td>-0.3 to 6.5 V</td>
<td>V</td>
</tr>
<tr>
<td>V_{LX}</td>
<td>L_{X} Pin Voltage</td>
<td>-0.3 to V_{IN} + 0.3 V</td>
<td>V</td>
</tr>
<tr>
<td>V_{OUT1}</td>
<td>V_{OUT1} Pin Voltage</td>
<td>-0.3 to V_{IN} + 0.3 V</td>
<td>V</td>
</tr>
<tr>
<td>V_{OUT2}</td>
<td>V_{OUT2} Pin Voltage</td>
<td>-0.3 to V_{IN} + 0.3 V</td>
<td>V</td>
</tr>
<tr>
<td>V_{DOUT}</td>
<td>V_{DOUT} Pin Voltage</td>
<td>-0.3 to 6.5 V</td>
<td>V</td>
</tr>
<tr>
<td>P_{D}</td>
<td>Power Dissipation*</td>
<td>(1) 1750 (Ta=25°C, T_{j,max}=150°C)</td>
<td>mW</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(2) 1138 (Ta=25°C, T_{j,max}=150°C)</td>
<td></td>
</tr>
<tr>
<td>Ta</td>
<td>Operating Temperature</td>
<td>-40 to +85 V</td>
<td>°C</td>
</tr>
<tr>
<td>T_{stg}</td>
<td>Storage Temperature</td>
<td>-55 to +125 V</td>
<td>°C</td>
</tr>
</tbody>
</table>

* For more information about Power Dissipation and Standard Land Pattern, refer to PACKAGE INFORMATION.

## ABSOLUTE MAXIMUM RATINGS

Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause the permanent damages and may degrade the life time and safety for both device and system using the device in the field. The functional operation at or over these absolute maximum ratings is not assured.

## RECOMMENDED OPERATING CONDITIONS (ELECTRICAL CHARACTERISTICS)

All of electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating conditions. The semiconductor devices cannot operate normally over the recommended operating conditions, even if when they are used over such conditions by momentary electronic noise or surge. And the semiconductor devices may receive serious damage when they continue to operate over the recommended operating conditions.
ELECTRICAL CHARACTERISTICS

Unless otherwise specified, the measurement is done by an open loop circuit. Unless otherwise specified, \( V_{IN} = V_{CE} = 5\, \text{V} \), AGND=PGND=0V.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{IN} )</td>
<td>Operating Input Voltage</td>
<td>( V_{IN} = V_{CE} = 5.5, \text{V} )</td>
<td>4.5</td>
<td>5.5</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>( I_{SS1} )</td>
<td>Supply Current 1</td>
<td>( V_{OUT1} = V_{SET} \times 0.8 )</td>
<td>460</td>
<td></td>
<td></td>
<td>( \mu\text{A} )</td>
</tr>
<tr>
<td>( I_{SS2} )</td>
<td>Supply Current 2 (applied to B/C/D version)</td>
<td>( V_{IN} = V_{CE} = 5.5, \text{V} )</td>
<td>170</td>
<td></td>
<td></td>
<td>( \mu\text{A} )</td>
</tr>
<tr>
<td>( I_{standby} )</td>
<td>Standby Current</td>
<td>( V_{IN} = 5.5, \text{V} )</td>
<td>1.00</td>
<td>2.0</td>
<td></td>
<td>( \mu\text{A} )</td>
</tr>
<tr>
<td>( V_{CEH} )</td>
<td>CE Input Voltage “H”</td>
<td>( V_{CE} = 0, \text{V} )</td>
<td>1.0</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( V_{CEL} )</td>
<td>CE Input Voltage “L”</td>
<td>( V_{CE} = 0, \text{V} )</td>
<td>0.3</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( T_{TSD} )</td>
<td>Thermal Shutdown Detector Temperature</td>
<td>Junction Temperature</td>
<td>165</td>
<td></td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td>( T_{TSR} )</td>
<td>Thermal Shutdown Release Temperature</td>
<td>Junction Temperature</td>
<td>110</td>
<td></td>
<td></td>
<td>°C</td>
</tr>
</tbody>
</table>

DC/DC SECTION (\( T_a = 25\, ^\circ\text{C} \))

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{OUT1} )</td>
<td>Output Voltage 1</td>
<td>( V_{IN} = 5, \text{V} )</td>
<td>-2.0%</td>
<td></td>
<td>+2.0%</td>
<td>V</td>
</tr>
<tr>
<td>( \Delta V_{OUT1} / \Delta T_a )</td>
<td>Output Voltage 1 Temperature Coefficient</td>
<td>(-40, ^\circ\text{C} \leq T_a \leq 85, ^\circ\text{C} )</td>
<td></td>
<td>±150</td>
<td></td>
<td>ppm/ °C</td>
</tr>
<tr>
<td>( f_{osc} )</td>
<td>Oscillator Frequency</td>
<td>( V_{IN} = 5, \text{V} )</td>
<td>-20%</td>
<td>1.2</td>
<td>+20%</td>
<td>MHz</td>
</tr>
<tr>
<td>( I_{LXLEAKH} )</td>
<td>Lx leakage Current “H”</td>
<td>( V_{IN} = V_{LX} = 5.5, \text{V}, V_{CE} = 0, \text{V} )</td>
<td>-1.0</td>
<td>0.0</td>
<td>5.0</td>
<td>( \mu\text{A} )</td>
</tr>
<tr>
<td>( I_{LXLEAKL} )</td>
<td>Lx leakage Current “L”</td>
<td>( V_{IN} = 5.5, \text{V}, V_{CE} = V_{LX} = 0, \text{V} )</td>
<td>-5.0</td>
<td>0.0</td>
<td>1.0</td>
<td>( \mu\text{A} )</td>
</tr>
<tr>
<td>( R_{ONP} )</td>
<td>P-channel transistor ON resistance</td>
<td>( V_{IN} = 5, \text{V}, I_{LX} = -100, \text{mA} )</td>
<td>0.25</td>
<td></td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td>( R_{ONN} )</td>
<td>N-channel transistor ON resistance</td>
<td>( V_{IN} = 5, \text{V}, I_{LX} = -100, \text{mA} )</td>
<td>0.25</td>
<td></td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td>Maxduty</td>
<td>Maximum Duty Cycle</td>
<td></td>
<td>100</td>
<td></td>
<td></td>
<td>%</td>
</tr>
<tr>
<td>tstart</td>
<td>Soft-start Time</td>
<td>( V_{IN} = V_{CE} = 5, \text{V} )</td>
<td>1.00</td>
<td></td>
<td></td>
<td>ms</td>
</tr>
<tr>
<td>( I_{LXlim} )</td>
<td>Lx Current Limit</td>
<td>( V_{IN} = V_{CE} = 5, \text{V} )</td>
<td>1.0</td>
<td>1.4</td>
<td></td>
<td>A</td>
</tr>
<tr>
<td>tprot</td>
<td>Protection Delay Time</td>
<td>( V_{IN} = V_{CE} = 5, \text{V} )</td>
<td>1.10</td>
<td>1.5</td>
<td></td>
<td>ms</td>
</tr>
<tr>
<td>( V_{UVLO1} )</td>
<td>UVLO Detector Threshold</td>
<td>( V_{IN} = V_{CE} )</td>
<td>3.40</td>
<td>3.50</td>
<td>3.60</td>
<td>V</td>
</tr>
<tr>
<td>( V_{UVLO2} )</td>
<td>UVLO Release Voltage</td>
<td>( V_{IN} = V_{CE} )</td>
<td>3.63</td>
<td>3.73</td>
<td>3.83</td>
<td>V</td>
</tr>
</tbody>
</table>

All test items listed under ELECTRICAL CHARACTERISTICS are done under the pulse load condition \( (T_j=Ta=25\, ^\circ\text{C}) \) except Thermal Shutdown.
### VR SECTION

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{OUT2}$</td>
<td>Output Voltage 2</td>
<td>$V_{IN}=5V$, $I_{OUT}=1mA$</td>
<td>-1.0%</td>
<td>+1.0%</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$I_{LIM2}$</td>
<td>Current Limit 2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>$I_{SS3}$</td>
<td>Supply Current 3</td>
<td>$V_{IN}=V_{CE}=5.5V$</td>
<td>60</td>
<td></td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td>$\Delta V_{OUT2}/\Delta I_{OUT2}$</td>
<td>Load Regulation</td>
<td>$1mA \leq I_{OUT2} \leq 400mA$</td>
<td>40</td>
<td>80</td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>$\Delta V_{OUT2}/\Delta T_a$</td>
<td>Output Voltage 2 Temperature Coefficient</td>
<td>$-40^\circ C \leq T_a \leq 85^\circ C$</td>
<td>±50</td>
<td></td>
<td></td>
<td>Ppm/°C</td>
</tr>
<tr>
<td>$I_{SC}$</td>
<td>Short Current Limit</td>
<td>$V_{OUT2}=0V$</td>
<td>70</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>$T_{VR}$ (A/B version)</td>
<td>Start-up Timing Delay</td>
<td>Start from the finish moment of soft start-time of DC/DC converter</td>
<td>2.0</td>
<td></td>
<td></td>
<td>ms</td>
</tr>
<tr>
<td>$T_{VR}$ (C/D Version)</td>
<td>Start-up Delay</td>
<td>Start from UVLO release moment of DC/DC converter</td>
<td>50</td>
<td></td>
<td></td>
<td>μs</td>
</tr>
<tr>
<td>$R_{LOW}$</td>
<td>For auto discharge at off, N-channel Tr. ON resistance</td>
<td>$V_{IN}=5V$, $V_{CE}=0V$</td>
<td>50</td>
<td></td>
<td></td>
<td>Ω</td>
</tr>
</tbody>
</table>

### VD SECTION

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$-V_{DET}$</td>
<td>VD Detector Threshold</td>
<td></td>
<td>-2.0%</td>
<td></td>
<td>+2.0%</td>
<td>V</td>
</tr>
<tr>
<td>$\Delta V_{DET}/\Delta T_a$</td>
<td>VD Detector Threshold Temperature Coefficient</td>
<td>$-40^\circ C \leq T_a \leq 85^\circ C$</td>
<td>±40</td>
<td></td>
<td></td>
<td>ppm/°C</td>
</tr>
<tr>
<td>$V_{HY}$</td>
<td>Hysteresis Range</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$T_{PLH}$</td>
<td>VD Release Delay Time</td>
<td></td>
<td>50</td>
<td></td>
<td></td>
<td>ms</td>
</tr>
<tr>
<td>$I_{DOUTL}$</td>
<td>$V_{DOUT}$ &quot;L&quot; Output Current</td>
<td>$V_{IN}=2.0V$, $V_{DOUT}=0.1V$</td>
<td>1.0</td>
<td>4.0</td>
<td></td>
<td>mA</td>
</tr>
</tbody>
</table>

All test items listed under **ELECTRICAL CHARACTERISTICS** are done under the pulse load condition ($T_j=T_a=25^\circ C$) except Thermal Shutdown.
TYPICAL APPLICATION AND TECHNICAL NOTES

External Components Recommendation
Inductor L1: 4.7 μH (A/B/C Version VLF4014AT-4R7M1R1 TDK)
  4.7 μH (D Version VLF4014ST-4R7M1R4 TDK)
Pull-up Resistance R1: 50kΩ
Capacitors C1: 10μF Ceramic capacitor (C2012JB0J106K TDK)
  C2: 2.2μF Ceramic capacitor
  C3: 10μF Ceramic capacitor (C2012JB0J106K TDK)

TECHNICAL NOTES ON EXTERNAL COMPONENTS

- Place all the external components as close as possible to the IC and make the wiring length as short as possible. Especially, the capacitor between V_IN and GND must be as close as possible to the IC. If the impedance of the power supply and ground is high, the power level of the IC may shift by the switching current and the operation may unstable. Make the power line and the ground line sufficient. Through the power line, the ground line, inductor, Lx pin, V_OUT line, large current may flow by switching, therefore fully consideration is necessary. The wiring between V_OUT pin and the inductor, and load and V_OUT pin must be separated.

- PVDD and AVDD must be short and make them close as possible. Place a capacitor as close as possible to PVDD. If the distance between AVDD and PVDD is long, add another 0.1μF capacitor between AVDD and GND.

- Capacitance value between VDD and GND should be 10μF or more and use a low ESR ceramic capacitor. Use a ceramic capacitor for V_OUT1 pin, and the capacitor should be 10μF or more. Use a ceramic capacitor for V_OUT2 pin, and the ceramic capacitor should be 2.2μF or more.

- Choose an inductor with low DCR, and enough permissible current and which is hard to reach magnetic saturation. If the inductance value is too small, at the maximum load, the current flows through Lx transistor and inductor may be beyond the absolute maximum rating. Choose an appropriate inductance value.

- If the spike noise of Lx pin is large, place a snubber circuit between Lx and GND (CR serial connection, etc.) to reduce the spike noise. Time constants of CR depend on the actual PCB and decide with the evaluation of the PCB.

- The performance of the power circuit with the IC depends on the peripheral circuits. In terms of the external components, PCB pattern, and IC, the peripheral circuit should be designed not to exceed beyond ratings (voltage, current, power).
STEP-DOWN DC/DC CONVERTERS’ OPERATION AND OUTPUT CURRENT

This explanation is about the general step-down DC/DC converters’ operation.

In the step-down DC/DC converter, when the Lx transistor turns on, at the same time, energy is accumulated into an inductor and when the transistor turns off, the current accumulated in the inductor is released and averaged, then make the energy loss reduced and the output voltage lower than the input voltage is supplied.

Step1. P-channel transistor turns on, current IL=i1, energy is charged into L, CL is charged and the output current IOUT is supplied. While the P-channel transistor turns on (tON), and in proportion to IL=i1 is from IL=ILmin=0 increases and reaches to ILmax.

Step2. P-channel transistor turns off, L keeps IL=ILmax, and turns on the N-channel transistor, current IL=i2 flows.

Step3. IL=i2 decreases gradually, after tOPEN, IL=ILmin=0 and N-channel transistor turns off.

However, if the cycle is continuous mode, before IL=ILmin=0, tOFF time becomes nothing, the next cycle starts and the P-channel transistor turns on, and the N-channel transistor turns off. In this case, ILmin >0 and charge is remained, and charge is increased from IL=ILmin >0.

In the PWM control, the number of switching in a second (fOSC) is fixed, and tON is controlled and the output voltage is constantly maintained.

The step-down operation is constant and stable, the current flows through the inductor’s maximum value (ILmax) and the minimum value (ILmin) is same as when the P-channel transistor turns on and off as described above. Supposed that the difference between ILmax and ILmin is ΔI,

\[ ΔI = IL\max - IL\min = \frac{V_{OUT} \times t_{OPEN}}{L} = \frac{(VIN - VOUT) \times t_{ON}}{L} \]

Thus,

\[ T = \frac{1}{f_{OSC}} = t_{ON} + t_{OFF} \]
\[ \text{duty (\%)} = \frac{t_{ON}}{T} \times 100 = \frac{t_{ON}}{f_{OSC}} \times 100 \]

The left side of the equation describes the current level at turning on, and the right side of the equation describes the current level at turning off.
OUTPUT CURRENT AND SELECTION OF EXTERNAL COMPONENTS

In the general step-down DC/DC converters, the relation between the output current and external components is described as below:

(Supposed that the peak to peak value of the ripple current is "IRP", On resistance of the LX transistor, P-channel transistor, N-channel transistor is respectively described as "RONP" and "RONN", inductor’s DCR is described as "RL")

Supposed that the time when LX P-channel transistor turns on is described as “tON”,

\[ V_{IN} = V_{OUT} + (RONP + RL) \times I_{OUT} + L \times IRP / tON \]  \hspace{1cm} \text{Formula 1}

Supposed that the time when LX P-channel transistor turns off (N-channel transistor turns on) is described as “tOFF”,

\[ L \times IRP / tOFF = (RONN + RL) \times I_{OUT} + V_{OUT} \]  \hspace{1cm} \text{Formula 2}

Using Formula 1 and Formula 2, and On duty of the P-channel transistor, \( tON / (tON + tOFF) = D_{ON} \) is solved,

\[ D_{ON} = (V_{OUT} + RONN \times I_{OUT} + RL \times I_{OUT}) / (V_{IN} - RONP \times I_{OUT} + RONN \times I_{OUT}) \]  \hspace{1cm} \text{Formula 3}

Ripple current is

\[ IRP = (V_{IN} - V_{OUT} - RONP \times I_{OUT} - RL \times I_{OUT}) \times D_{ON} / f_{OSC} / L \]  \hspace{1cm} \text{Formula 4}

Then the peak current through the inductor and LX transistor,

\[ I_{Lmax} = I_{OUT} + IRP / 2 \]  \hspace{1cm} \text{Formula 5}

Decide the peripheral circuits with considering ILmax and input and output conditions.

* The calculation is based on the ideal operation of the PWM continuous mode.
TIMING CHART (A Version)

(1) Start-up and shutdown by detecting UVLO

Timing chart of the power supply voltage change and DC/DC converter, VD, and VR can be explained as below:

(1) DC/DC converter
Power supply is forced and when VDD voltage increases, if VDD voltage is equal or less than the UVLO release voltage (VUVLO2), the operation of DC/DC converter stops and switching is halted, therefore the voltage, VOUT1 does not rise. When the VDD voltage becomes equal or more than UVLO release voltage, the DC/DC converter starts soft-start and switching begins and the voltage, VOUT1 rises. After the soft-start time, VDD voltage becomes set equal or more than VOUT1 voltage, VOUT1 voltage becomes set output voltage. When VDD voltage becomes equal or less than UVLO detector threshold (VUVLO1), DC/DC converter stops switching and turns off the Lx transistor inside the IC.

(2) VR
After the soft-start time of the DC/DC converter, VR starts up with delay time. The operation stops when VDD voltage becomes equal or less than UVLO detector threshold (VUVLO1), then auto-discharge function starts.

(3) VD
When VOUT2 voltage becomes equal or more than VD detector threshold voltage + hysteresis width (-VDET + VHYS), after the VD release delay time (TPLH), N-channel transistor of the IC turns off, VDOUT pin is pulled up with an external resistance and becomes pull-up voltage. When VDD voltage becomes equal or less than UVLO detector threshold (VUVLO1), then N-channel transistor of VDOUT pin turns on and VDOUT pin outputs "L". (Depending on VOUT1 or VOUT2, VDOUT pin outputs “L”. Refer to the timing chart.)
(2) Start-up and Turning off by detecting over current of DC/DC converter

Timing chart of DC/DC converter output change by load, VD and VR can be explained as below:

(1) DC/DC converter
When LX peak current (IOUT1) is beyond the current limit (ILXLIM),*1 the protection circuit operates and switching stops and Lx transistor inside the IC turns off and restarts after a certain time.

*1) During soft-start time, if IOUT1 is beyond ILXLIM, the protection circuit does not work.

(2) VR
When the DC/DC converter stops and at the same time, VR operation stops and auto-discharge function operates. To release it, after the soft-start time of the DC/DC converter, VR starts up with delay.

(3) VD
When the DC/DC converter stops and at the same time, the N-channel transistor of VDOUT pin turns on, VDOUT pin outputs “L”. To release it, when VOUT2 voltage becomes equal or more than VD detector threshold + hysteresis width (-VDET + VHYS), after VD release delay time (TPLH) the N-channel transistor inside the IC turns off and VDOUT pin becomes pull-up voltage by an external resistance.
(3) Start-up and Turning off by VR output decrease

Timing chart of turning off by VR output voltage decreases, DC/DC converter, VD and VR can be explained as below:

(1) DC/DC converter
DC/DC converter operates regardless of the operation of VR.

(2) VR
Since the short current limit is built-in, if the output is short to the GND or over-current flows, the output decreases with current limit. If the over current is released and set output voltage appears.

(3) VD
If VOUT2 becomes equal or less than VD detector threshold (-VDET), N-channel transistor of VDOUT pin turns on and VDOUT pin outputs "L". To release VD, when the voltage of VOUT2 becomes equal or more than VD detector threshold + hysteresis width (-VDET + VHY), after VD release delay time (TPLH), the N-channel transistor inside the IC turns off, VDOUT pin becomes pull-up voltage by an external resistance.
TIMING CHART (B Version)

Timing chart with Power supply change and DC/DC converter, VD and VR can be explained as below:

(1) DC/DC converter
Power supply is forced and VDD voltage increases, and if VDD voltage becomes equal or less than UVLO release voltage (VUVLO2), DC/DC converter operation stops and becomes no switching, therefore, VOUT1 voltage does not rise. When VDD voltage becomes equal or more than UVLO release voltage, the DC/DC converter starts soft-start and switching starts and VOUT1 voltage rises. After the soft-start time, if VDD voltage becomes equal or less than UVLO detector threshold (VUVLO1), the DC/DC converter stops switching and Lx transistor inside the IC turns off.

(2) VR
After the soft-start of DC/DC converter, VR starts up with delay. When the voltage of VDD becomes equal or less than UVLO detector threshold (VUVLO1), the operation stops and auto-discharge function starts.

(3) VD
VD operates regardless of the DC/DC converter, VR, thermal shutdown circuit, and chip-enable function. If the voltage of VDD becomes equal or less than VD detector threshold (−VDET), N-channel transistor of VDOUT pin turns on and VDOUT pin outputs "L". Then, when the voltage of VDD becomes equal or more than VD detector threshold + hysteresis width (−VDET + VHYS), after VD release delay time (TPLH), N-channel transistor inside the IC turns off and VDOUT pin becomes pull-up voltage by an external resistance.
Timing chart of the power supply change, DC/DC converter, VD, VR can be explained as below:

(1) DC/DC converter

Power supply is forced and when the voltage of VDD rises, the voltage of VDD is equal or less than UVLO release voltage (VUVLO2), DC/DC converter’s operation stops and becomes no switching, therefore the voltage of VOUT1 does not rise. When the voltage of VDD becomes equal or more than UVLO release voltage, DC/DC converter starts soft-start and switching begins and the voltage of VOUT1 rises. After soft-start time, if the voltage of VDD becomes equal or more than the set VOUT1 voltage, the output of VOUT1 becomes set output voltage. When the voltage of VDD becomes equal or less than UVLO detector threshold (VUVLO1), DC/DC converter stops switching, Lx transistor inside the IC turns off.

(2) VR

When the voltage of VDD becomes equal or more than UVLO release voltage, after the 30μs to 40μs or around, VR starts up. (Cout=2.2μF)
If the voltage of VDD becomes equal or less than UVLO detector threshold (VUVLO1), the operations stops and auto-discharge function operates.

(3) VD

VD operates regardless of DCDC, VR, thermal shutdown circuit, chip-enable function. When the voltage of VDD becomes or less than VD detector threshold (-VDET), N-channel transistor of VDOUT pin turns on, VDOUT pin outputs "L". Then when the voltage of VDD becomes equal or more than VD detector threshold + hysteresis width (-VDET + VHYs), after VD release delay time (TPLH), N-channel transistor inside the IC turns off, VDOUT pin becomes pull-up voltage by an externa resistance.
TEST CIRCUITS

Standby Current Test Circuit

Supply Current 1, 2 Test Circuit

DC/DC Output Voltage Test Circuit

DC/DC Oscillator Frequency Test Circuit

UVLO Detect and Release Voltage Test Circuit

VR Short Current Test Circuit

VD Detect and Release Voltage Test Circuit (for B, C, D Version)
TYPICAL CHARACTERISTIC
(unless otherwise specified, characteristics of C, D Version are same as B Version)

1) DC/DC output voltage vs. output current
   Version comparison

   **DC/DC output voltage vs. output current**
   - **Version comparison**
   - **VOUT1=1.2V VDD=5.0V**
     - Output Voltage [V]
     - Output Current [mA]
   - **VOUT1=1.8V VDD=5.0V**
     - Output Voltage [V]
     - Output Current [mA]

   **Input voltage comparison**
   - **VOUT1=1.5V A_Ver.**
     - Output Voltage [V]
     - Output Current [mA]
   - **VOUT1=1.5V B_Ver.**
     - Output Voltage [V]
     - Output Current [mA]

2) DC/DC output voltage vs. Input voltage

   **DC/DC output voltage vs. Input voltage**
   - **VOUT1=1.2V IOUT1=200mA**
   - **VOUT1=1.8V IOUT1=200mA**
3) Efficiency vs. Output current
   (1) Version comparison

   ![Efficiency vs. Output Current Graph A_Ver.](image)
   ![Efficiency vs. Output Current Graph B_Ver.](image)

(2) Input voltage comparison

   ![Efficiency vs. Output Current Graph A_Ver.](image)
   ![Efficiency vs. Output Current Graph B_Ver.](image)

4) Standby Current vs. Temperature

   ![Standby Current vs. Temperature](image)

5) Supply Current 1, 2, 3 vs. Temperature

   ![Supply Current vs. Temperature](image)
6) DC/DC output voltage vs. Temperature

![Graph showing DC/DC output voltage vs. Temperature for VOUT1=1.2V and VDD=5.0V.](image)

![Graph showing DC/DC output voltage vs. Temperature for VOUT1=1.8V and VDD=5.0V.](image)

7) Oscillator frequency vs. Temperature

![Graph showing Oscillator frequency vs. Temperature for VOUT1=1.5V and VDD=5.0V.](image)

8) Oscillator frequency vs. Input voltage

![Graph showing Oscillator frequency vs. Input voltage for VOUT1=1.5V and IOUT1=200mA.](image)

9) Soft-start time vs. Temperature

![Graph showing Soft-start time vs. Temperature for VOUT1=1.5V and VDD=5.0V.](image)

10) UVLO detect / release voltage vs. Input voltage

![Graph showing UVLO detect / release voltage vs. Temperature for VOUT1=1.5V.](image)
11) CE Input voltage vs. Temperature

\[ V_{OUT1} = 1.5V \quad V_{DD} = 5.0V \]

12) P-channel/N-channel Tr. ON resistance vs. Temperature

\[ V_{OUT1} = 1.5V \quad V_{DD} = 5.0V \]

13) Lx Current limit vs. Temperature (Version comparison)

\[ V_{OUT1} = 1.5V \quad V_{DD} = 5.0V \]

14) Protection delay time vs. Temperature (Version comparison)

\[ V_{OUT1} = 1.5V \quad V_{DD} = 5.0V \]

15) VR Output voltage vs. Temperature

\[ V_{OUT2} = 2.5V \quad I_{OUT2} = 1mA \quad V_{DD} = 5.0V \]

\[ V_{OUT2} = 3.3V \quad I_{OUT2} = 1mA \quad V_{DD} = 5.0V \]
16) VR Output voltage vs. Output current

![Graph of VR Output voltage vs. Output current for VOUT2=2.5V, VDD=5.0V](image1)

![Graph of VR Output voltage vs. Output current for VOUT2=3.3V, VDD=5.0V](image2)

17) VD detect/ release voltage vs. Temperature (Version comparison)

![Graph of VD detect/ release voltage vs. Temperature for A_Ver.](image3)

![Graph of VD detect/ release voltage vs. Temperature for B_Ver.](image4)

18) VDOUT “L” Output current vs. Temperature

![Graph of VDOUT “L” Output current vs. Temperature for VOUT2=0.1V, VDD=2.0V](image5)

19) Release delay time vs. Temperature

![Graph of Release delay time vs. Temperature for VOUT2=-3.0V, VDD=5.0V](image6)
20) DC/DC Output voltage waveform (Version comparison)
(CIN=Ceramic 10uF, COUT1= Ceramic 10uF, L=4.7uH, VDD=5.0V)

A Version

VOUT1=1.2V  IOUT1=10mA  A_Ver.

VOUT1=1.2V  IOUT1=400mA  A_Ver.

VOUT1=1.8V  IOUT1=10mA  A_Ver.

VOUT1=1.8V  IOUT1=400mA  A_Ver.

B Version

VOUT1=1.2V  IOUT1=10mA  B_Ver.

VOUT1=1.2V  IOUT1=400mA  B_Ver.
21) VOUT1, VOUT2 start-up waveform (Version comparison)
   (CIN=Ceramic 10uF, COUT1= Ceramic 10uF, COUT2= Ceramic 2.2uF, L=4.7uH)

A, B Version

C, D Version
22) **VDOUT Release Delay Waveform (Version comparison)**
(CIN=Ceramic 10uF, COUT1= Ceramic 10uF, COUT2= Ceramic 2.2uF, L=4.7uH)

\[ V_{OUT2}=2.5V \quad -V_{DET}=2.0V \quad A_{Ver.} \]

\[ V_{OUT2}=2.5V \quad -V_{DET}=3.0V \quad B_{Ver.} \]

23) **DC/DC Load transient response (Version comparison)**
(CIN=Ceramic 10uF, COUT1= Ceramic 10uF, L=4.7uH , VDD=5.0V)

A Version, **VOUT1=1.5V**

- **VOUT1=1.5V IOUT1=0mA to 400mA**
- **VOUT1=1.5V IOUT1=400mA to 0mA**
- **VOUT1=1.5V IOUT1=50mA to 500mA**
- **VOUT1=1.5V IOUT1=500mA to 50mA**
### B Version \( V_{OUT1} = 1.5V \)

- **\( V_{OUT1} = 1.5V \)  \( I_{OUT1} = 0mA \) to 400mA**
  - Output Voltage [V]: 1.30 to 1.55
  - Output Current [mA]: 0 to 400

- **\( V_{OUT1} = 1.5V \)  \( I_{OUT1} = 400mA \) to 0mA**
  - Output Voltage [V]: 1.30 to 1.55
  - Output Current [mA]: 400 to 0

- **\( V_{OUT1} = 1.5V \)  \( I_{OUT1} = 50mA \) to 500mA**
  - Output Voltage [V]: 1.30 to 1.55
  - Output Current [mA]: 50 to 500

- **\( V_{OUT1} = 1.5V \)  \( I_{OUT1} = 500mA \) to 50mA**
  - Output Voltage [V]: 1.30 to 1.55
  - Output Current [mA]: 500 to 50
24) VR Load transient response (DC/DC load current comparison)
(CIN=Ceramic 10uF, COUT2= Ceramic 2.2uF, VDD=5.0V)

DC/DC load current IOUT2=0mA

DC/DC load current IOUT2=400mA
POWER DISSIPATION-(1) / DFN(PLP)2527-10

DFN(PLP)2527-10 package power dissipation characteristic is shown below. The power dissipation depends on the conditions of the mounting on PCB and this is just an example.

**Test conditions**

<table>
<thead>
<tr>
<th>Test Condition</th>
<th>Standard Mounting on Board Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Board material</td>
<td>Glass Epoxy Resin (4-layer)</td>
</tr>
<tr>
<td>Board dimensions</td>
<td>35mm x 90mm x 0.8mm</td>
</tr>
<tr>
<td>Wiring ratio</td>
<td>Each layer 15%</td>
</tr>
<tr>
<td>Cupper wire thickness</td>
<td>Top/Bottom layer: 35μm, Middle layer: 18μm</td>
</tr>
<tr>
<td>Through holes</td>
<td>9(φ0.3mm) package tab connection land pattern, from top to bottom 10 (φ0.5mm) for each pin connection</td>
</tr>
</tbody>
</table>

**Measurement result**

<table>
<thead>
<tr>
<th>Power Dissipation Conditions</th>
<th>Standard Mounting on Board Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Dissipation</td>
<td>1400mW (Tjmax=125°C)</td>
</tr>
<tr>
<td></td>
<td>1750mW (Tjmax=150°C)</td>
</tr>
<tr>
<td>Thermal Resistance</td>
<td>$\theta_{ja} = (125-25°C) / 1.4W \ 71°C / W$</td>
</tr>
</tbody>
</table>

* The hatched area usage has some impact on the product life time. The time for the usage of the hatched area should be less than 13,000 hours. If four hours a day, the product is used, the time limit is 9 years.*
POWER DISSIPATION-(2) / DFN(PLP)2527-10

DFN(PLP)2527-10 package another typical characteristic is shown below.

Test Conditions

<table>
<thead>
<tr>
<th>Test condition</th>
<th>Mounting on Board Conditions (2)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Board material</td>
<td>Glass Epoxy Resin (Printed on both sides)</td>
</tr>
<tr>
<td>Board dimensions</td>
<td>40mm × 40mm × 1.6mm</td>
</tr>
<tr>
<td>Wiring ratio</td>
<td>Top side 50%, Bottom side 50%</td>
</tr>
<tr>
<td>Through holes</td>
<td>Diameter 0.54mm × 30 pcs</td>
</tr>
</tbody>
</table>

Measurement result

<table>
<thead>
<tr>
<th>Power dissipation Characteristics</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power dissipation</td>
</tr>
<tr>
<td>910mW (Tjmax=125°C)</td>
</tr>
<tr>
<td>1138mW (Tjmax=150°C)</td>
</tr>
<tr>
<td>Thermal resistance</td>
</tr>
<tr>
<td>$\theta_{ja} = (125-25°C) / 0.91W = 110°C /W$</td>
</tr>
</tbody>
</table>

Power Dissipation Characteristic

$\theta_{ja}$

Mounting on Board Conditions (2)

<table>
<thead>
<tr>
<th>Power dissipation</th>
<th>Power dissipation Characteristics</th>
</tr>
</thead>
<tbody>
<tr>
<td>910mW (Tjmax=125°C)</td>
<td></td>
</tr>
<tr>
<td>1138mW (Tjmax=150°C)</td>
<td></td>
</tr>
</tbody>
</table>

* $T_{jmax}=125°C$ and $T_{jmax}=150°C$ Power dissipation characteristics are shown in the graph. The hatched area usage has some impact on the product lifetime. Time limit is described in the next table.

<table>
<thead>
<tr>
<th>Time limit</th>
<th>Product life time (4hours/day usage)</th>
</tr>
</thead>
<tbody>
<tr>
<td>13,000 hrs</td>
<td>9 years</td>
</tr>
</tbody>
</table>

Test Board Layout

IC mount position (Unit: mm)
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