OUTLINE

The R1270S is CMOS-based Step-down DC/DC converter with internal N-channel high side Tr. The ON resistance of the built-in high-side transistor is 0.10Ω and the R1270S can provide the maximum 3 A output current. Each of the ICs consists of an oscillator, a PWM control circuit, a voltage reference unit, an error amplifier, a phase compensation circuit, a slope compensation circuit, a soft-start circuit, protection circuits, an internal voltage regulator, and a switch for bootstrap circuit. The ICs can make up a step-down DC/DC converter with adding an inductor, resistors, a diode, and capacitors externally. The R1270S is current mode operating type DC/DC converters without an external current sense resistor, and realizes fast response and high efficiency. As an output capacitor, a ceramic type capacitor is usable. The internal oscillator frequency is adjustable over a range of 300 kHz to 2400 kHz by an external resistor, and also can be synchronized externally by PLL. The phase compensation is adjustable by using external resistor and capacitor. Thereby optimizations for the inductor and the capacitor can be done. To improve performance under light load conditions, the R1270S can select automatically between two modes: the VFM mode when the inductor current is discontinuous and the PWM mode when the inductor current is continuous. The ripple voltage at VFM mode is 40 mV (Typ.). As for protection, the R1270S has a current limit function to control an inductor peak current every a cycle, a fold-back function to reduce the oscillator frequency under the short circuit, a thermal shutdown function, an under voltage lockout (UVLO) function, and an over voltage lockout (OVLO) function. Furthermore, the R1270S can include a latch protection function to cut off the output when the output current reaches the set current limit for a certain time. That is, the R1270S supports two types of the presence (R1270S001A) or the absence (R1270S001B) of the latch protection function. The current limit, which is fixed at 4.5 A (Typ.), is adjustable by an external resistor. And, the soft start time is fixed at 0.4 ms (Typ.) internally, but is adjustable by an external resistor. The R1270S has the FLG pin to monitor the overvoltage of the FB pin voltage and the 6 V rated pin. When detecting an abnormal voltage, the R1270S outputs a flag. The R1270S is available in HSOP-18 package.
FEATURES

- Operating Voltage (Maximum Rating): 3.6 V to 34 V (36 V)
- Consumption Current: Typ. 18 µA (VIN = 12 V)
- Stand-by Current: Typ. 0 µA (VIN = 34 V, CE = 0 V)
- Output Voltage: Externally-adjustable at 0.8 V or more
  (Max. step down ratio 160 ns \( \times \) fosc)
- Feedback Voltage and Tolerance: 0.8 V ± 1.0%
- Output Current: 3 A\(^{(1)}\)
- Operating Frequency: 300 kHz to 2.4 MHz settable by External resistor
- Minimum Off Time: Typ. 120 ns
- Maximum Duty: Min. 93% (fosc = 300 kHz), Min. 67% (fosc = 2400 kHz)
- UVLO Function Detection Voltage: Typ. 2.6 V
- OVLO Function Detection Voltage: Min. 38 V
- Soft-start Time: Internal soft-start time (Typ. 0.4 ms), as a lower limit,
  Externally-adjustable by using capacitor
- High-side Switch Current Limit: Typ. 4.5 A, as an upper limit,
  Externally-adjustable by using resistor
- Thermal Shutdown Function: Typ. 160°C
- CE Threshold Voltage: Typ. 1.0 V
- Latch Protection Delay Time: Typ. 2 ms (R1270S001A)
- Fold-back Protection: Fold-back for Oscillation frequency
- \( V_{FB} \) Voltage Temperature Tolerance (\( \Delta V_{FB}/\Delta T_a \)): Typ. ±100 ppm/°C (−40°C ≤ \( T_a \) ≤ 105°C)
- Packages: HSOP-18

APPLICATIONS

- Power source for digital home appliances such as digital TV, DVD players.
- Power source for office equipment such as printers and fax machines.
- Power source for 5 V PSU or 2-cell or more Li-ion battery powered communication equipment, cameras, video instruments such as VCRs, camcorders.
- Power source for high voltage battery-powered equipment.

\(^{(1)}\) The output current depends on external components and conditions.
SELECTION GUIDE
The latch type protection function is user-selectable.

Selection Guide

<table>
<thead>
<tr>
<th>Product Name</th>
<th>Package</th>
<th>Quantity per Reel</th>
<th>Pb Free</th>
<th>Halogen Free</th>
</tr>
</thead>
<tbody>
<tr>
<td>R1270S001+-E2-FE</td>
<td>HSOP-18</td>
<td>1,000 pcs</td>
<td>Yes</td>
<td>Yes</td>
</tr>
</tbody>
</table>

*: Select the presence or absence of the latch type protection function.
A: with Latch type protection function
B: without Latch type protection function

BLOCK DIAGRAMS

R1270S001A/B Block Diagram

(1) R1270S001A equips the limit latch circuit.
<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1, 2</td>
<td>LX</td>
<td>Lx Switching Pin</td>
</tr>
<tr>
<td>3</td>
<td>NC</td>
<td>No connection</td>
</tr>
<tr>
<td>4</td>
<td>GND</td>
<td>Ground Pin</td>
</tr>
<tr>
<td>5</td>
<td>INT</td>
<td>Internal Bias Pin</td>
</tr>
<tr>
<td>6</td>
<td>FB</td>
<td>Feedback Pin</td>
</tr>
<tr>
<td>7</td>
<td>ER</td>
<td>Phase Compensation Pin for External Resistor</td>
</tr>
<tr>
<td>8</td>
<td>EC</td>
<td>Phase Compensation Pin for External Capacitor</td>
</tr>
<tr>
<td>9</td>
<td>LMT</td>
<td>Current Limit adjustment Pin</td>
</tr>
<tr>
<td>10</td>
<td>PLLREF</td>
<td>PLL Synchronization Pin</td>
</tr>
<tr>
<td>11</td>
<td>PLLFLTR</td>
<td>PLL Filter Pin</td>
</tr>
<tr>
<td>12</td>
<td>RT</td>
<td>Oscillation adjustment Pin</td>
</tr>
<tr>
<td>13</td>
<td>FLG</td>
<td>Flag Output Pin</td>
</tr>
<tr>
<td>14</td>
<td>CE</td>
<td>Chip Enable Pin (Active “H”)</td>
</tr>
<tr>
<td>15</td>
<td>SS</td>
<td>Soft-start Pin</td>
</tr>
<tr>
<td>16</td>
<td>BST</td>
<td>Bootstrap Pin</td>
</tr>
<tr>
<td>17, 18</td>
<td>VIN</td>
<td>Power Supply Pin</td>
</tr>
</tbody>
</table>

* The tab on the bottom of the package must be electrically connected to GND (substrate level) when mounted on the board.
Internal Equivalent Circuits for Individual Pins

Lx Pin Internal Equivalent Circuit

INT Pin Internal Equivalent Circuit

FB Pin Internal Equivalent Circuit

ER Pin Internal Equivalent Circuit

EC Pin Internal Equivalent Circuit

LMT Pin Internal Equivalent Circuit
BST Pin Internal Equivalent Circuit
### ABSOLUTE MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Item</th>
<th>Rating</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IN}$</td>
<td>Input Voltage</td>
<td>$-0.3$ to $36$</td>
<td>V</td>
</tr>
<tr>
<td>$V_{BST}$</td>
<td>BST Pin Voltage$^{(1)}$</td>
<td>$V_{LX} - 0.3$ to $V_{LX} + 6$</td>
<td>V</td>
</tr>
<tr>
<td>$V_{LX}$</td>
<td>LX Pin Voltage</td>
<td>$-0.3$ to $36$</td>
<td>V</td>
</tr>
<tr>
<td>$V_{CE}$</td>
<td>CE Pin Input Voltage</td>
<td>$-0.3$ to $36$</td>
<td>V</td>
</tr>
<tr>
<td>$V_{INT}$</td>
<td>INT Pin Voltage</td>
<td>$-0.3$ to $36$</td>
<td>V</td>
</tr>
<tr>
<td>$V_{SS}$</td>
<td>Soft-start Pin Voltage</td>
<td>$-0.3$ to $6$</td>
<td>V</td>
</tr>
<tr>
<td>$V_{ER}$</td>
<td>ER Pin Voltage</td>
<td>$-0.3$ to $6$</td>
<td>V</td>
</tr>
<tr>
<td>$V_{EC}$</td>
<td>EC Pin Voltage</td>
<td>$-0.3$ to $6$</td>
<td>V</td>
</tr>
<tr>
<td>$V_{FB}$</td>
<td>Feedback Pin Voltage</td>
<td>$-0.3$ to $6$</td>
<td>V</td>
</tr>
<tr>
<td>$V_{FLG}^{(1)}$</td>
<td>Flag Pin Voltage$^{(1)}$</td>
<td>$-0.3$ to $24$</td>
<td>V</td>
</tr>
<tr>
<td>$V_{PLLREF}$</td>
<td>External Oscillation Synchronization Pin Voltage</td>
<td>$-0.3$ to $36$</td>
<td>V</td>
</tr>
<tr>
<td>$V_{PLLFLTR}$</td>
<td>PLL Filter Pin Voltage</td>
<td>$-0.3$ to $6$</td>
<td>V</td>
</tr>
<tr>
<td>$V_{RT}$</td>
<td>Oscillation adjustment Pin Voltage</td>
<td>$-0.3$ to $6$</td>
<td>V</td>
</tr>
<tr>
<td>$V_{LMT}$</td>
<td>Current Limit adjustment Pin Voltage</td>
<td>$-0.3$ to $6$</td>
<td>V</td>
</tr>
<tr>
<td>$P_D$</td>
<td>Power Dissipation$^{(2)}$ (HSOP-18, JEDEC STD.51)</td>
<td>3100</td>
<td>mW</td>
</tr>
<tr>
<td>$T_j$</td>
<td>Junction Temperature Range</td>
<td>$-40$ to $125$</td>
<td>°C</td>
</tr>
<tr>
<td>$T_{stg}$</td>
<td>Storage Temperature Range</td>
<td>$-55$ to $125$</td>
<td>°C</td>
</tr>
</tbody>
</table>

ABSOLUTE MAXIMUM RATINGS

Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause permanent damage and may degrade the life time and safety for both device and system using the device in the field. The functional operation at or over these absolute maximum ratings are not assured.

### RECOMMENDED OPERATING CONDITIONS

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Item</th>
<th>Rating</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IN}$</td>
<td>Input Voltage</td>
<td>3.6 to 34</td>
<td>V</td>
</tr>
<tr>
<td>$T_a$</td>
<td>Operating Temperature</td>
<td>$-40$ to $105$</td>
<td>°C</td>
</tr>
</tbody>
</table>

RECOMMENDED OPERATING CONDITIONS

All of electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating conditions. The semiconductor devices cannot operate normally over the recommended operating conditions, even if they are used over such conditions by momentary electronic noise or surge. And the semiconductor devices may receive serious damage when they continue to operate over the recommended operating conditions.

---

$^{(1)}$ The pin voltage except $V_{BST}$ and $V_{FLG}$ must be prevented from exceeding $V_{IN} + 0.3V$.

$^{(2)}$ Refer to POWER DISSIPATION for detailed information.
### ELECTRICAL CHARACTERISTICS

$V_{IN} = 12\,\text{V},\, Ta = 25^\circ\text{C}$, unless otherwise specified.

The specifications surrounded by [ ] are guaranteed by design engineering at $-40^\circ\text{C} \leq Ta \leq 105^\circ\text{C}$.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Item</th>
<th>Conditions</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{IN}$</td>
<td>$V_{IN}$ Consumption current 1</td>
<td>$V_{IN} = 34,\text{V},, V_{INT} = \text{Open},, V_{PLLREF} = 34,\text{V},, V_{FB} = 1.5,\text{V}$</td>
<td>0.7</td>
<td>1</td>
<td>1.3</td>
<td>mA</td>
</tr>
<tr>
<td>$I_{IN}$</td>
<td>$V_{IN}$ Consumption current 2</td>
<td>$V_{IN} = 34,\text{V},, V_{INT} = \text{Open},, V_{PLLREF} = 0,, V_{FB} = 0.84,\text{V}$</td>
<td>13</td>
<td>18</td>
<td>30</td>
<td>$\mu\text{A}$</td>
</tr>
<tr>
<td>$V_{UVLO2}$</td>
<td>UVLO Released Voltage</td>
<td>$V_{IN}$ Rising</td>
<td>2.5</td>
<td>2.6</td>
<td>2.7</td>
<td>V</td>
</tr>
<tr>
<td>$V_{UVLO1}$</td>
<td>UVLO Detect Voltage</td>
<td>$V_{IN}$ Falling</td>
<td>$V_{UVLO2} = -0.15$</td>
<td>$V_{UVLO2} = -0.11$</td>
<td>$V_{UVLO2} = -0.15$</td>
<td>V</td>
</tr>
<tr>
<td>$V_{OVLO2}$</td>
<td>OVLO Released Voltage</td>
<td>$V_{IN}$ Falling</td>
<td>34</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{OVLO1}$</td>
<td>OVLO Detect Voltage</td>
<td>$V_{IN}$ Rising</td>
<td>38</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{FB}$</td>
<td>$V_{FB}$ Voltage Tolerance</td>
<td>$Ta = 25^\circ\text{C}$</td>
<td>0.792</td>
<td>0.800</td>
<td>0.808</td>
<td>V</td>
</tr>
<tr>
<td> </td>
<td> </td>
<td>$-40^\circ\text{C} \leq Ta \leq 105^\circ\text{C}$</td>
<td>0.784</td>
<td>0.816</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{VFM}$</td>
<td>FB High Detection at VFM mode</td>
<td></td>
<td>0.831</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$f_{osc0}$</td>
<td>Oscillation Frequency 0</td>
<td>RT = Open</td>
<td>270</td>
<td>300</td>
<td>330</td>
<td>kHz</td>
</tr>
<tr>
<td>$f_{osc1}$</td>
<td>Oscillation Frequency 1</td>
<td>RT = 62 k$\Omega$</td>
<td>900</td>
<td>1010</td>
<td>1120</td>
<td>kHz</td>
</tr>
<tr>
<td>$f_{osc2}$</td>
<td>Oscillation Frequency 2</td>
<td>RT = GND</td>
<td>2160</td>
<td>2400</td>
<td>2640</td>
<td>kHz</td>
</tr>
<tr>
<td>$t_{off}$</td>
<td>Minimum Off Time</td>
<td></td>
<td>120</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$D_{MAX0}$</td>
<td>Maximum Duty Cycle 0</td>
<td>RT = Open</td>
<td>93</td>
<td></td>
<td></td>
<td>%</td>
</tr>
<tr>
<td>$D_{MAX0}$</td>
<td>Maximum Duty Cycle 1</td>
<td>RT = 62 k$\Omega$</td>
<td>93</td>
<td></td>
<td></td>
<td>%</td>
</tr>
<tr>
<td>$D_{MAX2}$</td>
<td>Maximum Duty Cycle 2</td>
<td>RT = GND</td>
<td>87</td>
<td></td>
<td></td>
<td>%</td>
</tr>
<tr>
<td>$f_{SYNC}$</td>
<td>Oscillation Synchronized Frequency</td>
<td>$f_{PLLREF} = 1000,\text{kHz}$</td>
<td>$f_{osc}/2$</td>
<td></td>
<td></td>
<td>kHz</td>
</tr>
<tr>
<td>$t_{ss1}$</td>
<td>Soft-start Time 1</td>
<td>SS = Open, $V_{FB} = 0.72,\text{V}$</td>
<td>3.3</td>
<td></td>
<td>5.5</td>
<td>ms</td>
</tr>
<tr>
<td>$t_{ss2}$</td>
<td>Soft-start Time 2</td>
<td>CSS = 0.01 $\mu\text{F},, V_{FB} = 0.72,\text{V}$</td>
<td>3.1</td>
<td></td>
<td>4.5</td>
<td>ms</td>
</tr>
<tr>
<td>$t_{ltss}$</td>
<td>Soft-start charge current</td>
<td>SS = 0 V</td>
<td>1.7</td>
<td>2.0</td>
<td>2.35</td>
<td>$\mu\text{A}$</td>
</tr>
<tr>
<td>$t_{delay}$</td>
<td>Delay Time for Latch Protection</td>
<td>for R1270S001A</td>
<td>1.4</td>
<td>2</td>
<td>2.8</td>
<td>ms</td>
</tr>
<tr>
<td>$R_{LXH}$</td>
<td>Lx High Side Switch ON Resistance</td>
<td>$V_{BST} - V_{LX} = 4.5,\text{V},, I_{LX} = 0.1,\text{A}$</td>
<td>0.1</td>
<td></td>
<td>0.15</td>
<td>$\Omega$</td>
</tr>
<tr>
<td>$I_{LXHOFF}$</td>
<td>Lx High Side Switch Leakage Current</td>
<td></td>
<td>0</td>
<td></td>
<td>20</td>
<td>$\mu\text{A}$</td>
</tr>
<tr>
<td>$I_{LIMLX1}$</td>
<td>Lx High Side Switch Limited Current 1</td>
<td>$LMT = 220,\text{k}$, DC Current</td>
<td>3.0</td>
<td>3.5</td>
<td>4.3</td>
<td>A</td>
</tr>
<tr>
<td>$I_{LIMLX2}$</td>
<td>Lx High Side Switch Limited Current 2</td>
<td>$LMT = 39,\text{k}$, DC Current</td>
<td>1.25</td>
<td>1.6</td>
<td>2.4</td>
<td>A</td>
</tr>
</tbody>
</table>

All test items listed under Electrical Characteristics are done under the pulse load condition ($Tj = Ta = 25^\circ\text{C}$).
**ELECTRICAL CHARACTERISTICS (continued)**

$V_{IN} = 12$ V, $Ta = 25^\circ$C, unless otherwise specified.

The specifications surrounded by [ ] are guaranteed by design engineering at $-40^\circ$C $\leq Ta \leq 105^\circ$C.

### R1270S001A/B Electrical Characteristics (Ta = 25°C)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Item</th>
<th>Conditions</th>
<th>Conditions</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{CEH}$</td>
<td>CE “H” Input Voltage</td>
<td></td>
<td></td>
<td>1.15</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{CEL}$</td>
<td>CE “L” Input Voltage</td>
<td></td>
<td></td>
<td>0.85</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$I_{CEH}$</td>
<td>CE “H” Input Current</td>
<td>$V_{FB} = 1.5$ V</td>
<td></td>
<td>$-0.1$</td>
<td>0</td>
<td>$0.1$</td>
<td>µA</td>
</tr>
<tr>
<td>$I_{CEL}$</td>
<td>CE “L” Input Current</td>
<td></td>
<td></td>
<td>$-0.1$</td>
<td>0</td>
<td>$0.1$</td>
<td>µA</td>
</tr>
<tr>
<td>$I_{FBL}$</td>
<td>FB “H” Input Current</td>
<td>$V_{FB} = 0$ V</td>
<td></td>
<td>$-0.1$</td>
<td>0</td>
<td>$0.1$</td>
<td>µA</td>
</tr>
<tr>
<td>$I_{FBL}$</td>
<td>FB “L” Input Current</td>
<td></td>
<td></td>
<td>$-0.1$</td>
<td>0</td>
<td>$0.1$</td>
<td>µA</td>
</tr>
<tr>
<td>$V_{PLLH}$</td>
<td>PLLREF “H” Input Voltage</td>
<td></td>
<td></td>
<td>0.95</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{PLLL}$</td>
<td>PLLREF “L” Input Voltage</td>
<td></td>
<td></td>
<td>0.67</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$I_{PLLH}$</td>
<td>PLLREF “H” Input Current</td>
<td>$V_{FB} = 1.5$ V</td>
<td></td>
<td>$-0.1$</td>
<td>0</td>
<td>$0.1$</td>
<td>µA</td>
</tr>
<tr>
<td>$I_{PLLL}$</td>
<td>PLLREF “L” Input Current</td>
<td></td>
<td></td>
<td>$-0.1$</td>
<td>0</td>
<td>$0.1$</td>
<td>µA</td>
</tr>
<tr>
<td>$T_{TSD}$</td>
<td>Thermal Shutdown Detect Temperature</td>
<td></td>
<td></td>
<td>160</td>
<td></td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>$T_{TSR}$</td>
<td>Thermal Shutdown Release Temperature</td>
<td></td>
<td></td>
<td>130</td>
<td></td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>$I_{standby}$</td>
<td>Standby Current</td>
<td>$V_{IN} = 34$ V, $V_{CE} = 0$ V</td>
<td></td>
<td>0</td>
<td></td>
<td>20</td>
<td>µA</td>
</tr>
<tr>
<td>$V_{FLGL}$</td>
<td>FLAG “L” Voltage</td>
<td>$V_{IN} = 2.0$ V, $I_{FLG} = 1$ mA</td>
<td></td>
<td></td>
<td></td>
<td>0.23</td>
<td>V</td>
</tr>
<tr>
<td>$I_{FLGOFF}$</td>
<td>FLAG “Off” Current</td>
<td>$V_{FLG} = 6.0$ V</td>
<td></td>
<td></td>
<td></td>
<td>0.0</td>
<td>0.1</td>
</tr>
<tr>
<td>$V_{OVP}$</td>
<td>FB Pin OVP Detect Voltage</td>
<td></td>
<td></td>
<td>0.91</td>
<td>0.98</td>
<td>1.04</td>
<td>V</td>
</tr>
<tr>
<td>$V_{UVD}$</td>
<td>FB Pin UVD Detect Voltage</td>
<td></td>
<td></td>
<td>0.59</td>
<td>0.64</td>
<td>0.69</td>
<td>V</td>
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<tr>
<td>$V_{FBL}$</td>
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<tr>
<td>$V_{POVD}$</td>
<td>6V-rated Pin OVP Detect Voltage</td>
<td>$V_{ER}, V_{PLLFLTR}, V_{SS}$</td>
<td></td>
<td></td>
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<td>$V_{VOS0}$</td>
<td>INT Pin Operation Voltage</td>
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<tr>
<td>$V_{VOS1}$</td>
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<td></td>
<td>2.68</td>
<td>2.8</td>
<td></td>
<td>V</td>
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</tbody>
</table>

All test items listed under Electrical Characteristics are done under the pulse load condition ($T_j = Ta = 25^\circ$C).
THEORY OF OPERATION

OVLO (Over Voltage Lock Out) Function
When the input voltage to VIN pin is higher than OVLO detection voltage, the inside circuit becomes standby to prevent malfunction. If the voltage on the VIN pin becomes lower than the OVLO release voltage, R1270S will restart and the soft-start function will begin. Also, the OVLO protection has a function to prevent the possibility of the malfunction and destruction to the IC. Since the OVLO detection voltage is set higher than the absolute maximum rating for VIN pin, the function itself is not guaranteed.

OVP (Over Voltage Protection) Function for FB Pin
When the FB pin voltage becomes higher than the OVP detection voltage, the OVP function stops the switching of Lx pin without stopping the function of the internal circuit. When the FB pin voltage becomes lower than the OVP detect voltage, the Lx pin switching returns to normal control. If aberrant conditions around the FB pin circuit occur, the overvoltage of the output voltage may not be decreased because the R1270S indirectly monitors the output voltage via FB pin.

Setup for Oscillation Frequency
By using RRT between the RT pin and GND, the R1270S can control the oscillation frequency in the range of 300 kHz to 2400 kHz. For example, by using 62 kΩ as RRT, the frequency will be set about 1000 kHz.
When setting the frequency at either 300 kHz or 2400 kHz, the frequency depends on whether the RT pin is set to "Open" or "GND", without using RRT. That is, the frequency is set at 300 kHz when the RT pin is "Open", and is set at 2400 kHz when it is "GND".
The Electrical Characteristics guarantees the oscillation frequency under the conditions stated below for fOCS0, fOCS1 and fOCS2.

\[ R_{RT} [kΩ] = \frac{1}{(1 / ((1 / fosc [kHz]) x 1000000 - 125) / 292 x 25) - 25) - 1 / 250} \]

R1270S001A/B Oscillation Frequency Setting Resistor (RRT) vs. Oscillation Frequency (fosc)
Synchronization of Oscillation Frequency

The R1270S can synchronize to an external clock, which is input from the PLLREF pin, with using phase-locked loop. The PWM fixed mode is set during synchronization. The detection threshold of the external clock is 0.8 V (Typ.) and the pulse of 100 ns or more are required.

The phase compensation filter is required to stabilize the phase-locked loop. The frequency fluctuation, which is changed from the set frequency to the synchronized frequency, can be achieved smoothly by the constant of this filter. Place 10 kΩ resistor and 220 pF capacitor in series between PLLFTR pin and GND.

The oscillation frequency which could be synchronized is 0.5 to 2 times of that stated in the “Setup of Oscillation Frequency”. However the guaranteed oscillation frequency is 270 kHz at the minimum, and 2640 kHz at the maximum. Until the soft-start sequence is over, the R1270S operates at set oscillation frequency and after the soft-start sequence is over the oscillation frequency is synchronized to the external clock.

The phase compensation filter is charged with limited impedance, and the filter must be charged when synchronization starts. The time required for the phase compensation filter to be charged is as bellow.

$$\text{POLE}_{PLL} = 1/(C_{PLL} \cdot (R_{PLL} + 260\,\text{kΩ}))$$

95% charged : \(3/\text{POLE}_{PLL}\) [sec]
98% charged : \(4/\text{POLE}_{PLL}\) [sec]

Adjust the soft-start time or the timing of the external clock input as \(\text{POLE}_{PLL}\). The following shows the timing chart of self oscillation and external clock input.
VFM/PWM Alternative Mode and PWM Fixed Mode

By applying either the voltage of 0.95 V or more or the external clock to the PLLREF pin, the R1270S operates in PWM fixed mode (Pulse-skip at light load). By applying the voltage of 0.67 V or less to the PLLREF pin, the R1270S operates in VFM/PWM alternative mode.

INT Pin Voltage

By applying the voltage of 3.1 V (Typ.) or more to the INT pin via the VOUT pin, the R1270S generates 3 V internal power supply from VOUT. Thereby the R1270S can improve the efficiency of the IC in VFM mode. When IIN_VFM is as the 3 V internal current supply, the approximate expression for IC’s consumption current: IN is VOUT / VIN × IIN_VFM. That is, the consumption current will decrease as VOUT/VIN becomes smaller. But, when the INT pin voltage is lower than 3.1 V, the consumption current will not be reduced since the internal voltage supply becomes VIN. Therefore, this architecture is aimed for applications which the VOUT is 3.3 V or more. If the VOUT is lower than 3.3 V, set the INT pin OPEN (No CINT necessary).
Minimum ON Time
The minimum ON time is 160 ns that is determined by the current sense circuit. The R1270S adopts a resistor free current control mode. By using $R_{\text{ON}}$ (Nch driver ON resistor) as a substitute for sense resistor, the R1270S senses $I_L$ (inductor current) according to $V_{\text{IN}} - V_{\text{LX}} = I_L \times R_{\text{ON}}$. The R1270S can sense $I_L$ only during the Nch driver is On ($L_x = \text{“High”}$). However, if sensing it during the occurrence of the surge current right after the driver turns On, a malfunction may occur. To avoid the malfunction, the R1270S maintains a none sensing time for a while after the driver turns On.

If the current control mode and the current limit circuit will not function properly at none sensing time, the R1270S may result in a rapid deterioration of stability and current limit accuracy. Please select the output voltage settings and frequency settings so that the output voltage does not become lower than the minimum step down ratio:

$$V_{\text{IN}} \times 160 \text{ ns} \times f_{\text{OCS}}.$$

CSPD Setting
The transfer function from feedback resistor of $V_{\text{OUT}}$ to FB pin using $C_{\text{SPD}}$ is

$$V_{\text{OUT}} / FB [s] = (R_{\text{TOP}} \times R_{\text{BOT}} \times C_{\text{SPD}} \times s + R_{\text{BOT}}) / (R_{\text{TOP}} \times R_{\text{BOT}} \times C_{\text{SPD}} \times s + R_{\text{TOP}} + R_{\text{BOT}}).$$

From above equation, the zero is $R_{\text{BOT}} / (R_{\text{TOP}} \times R_{\text{BOT}} \times C_{\text{SPD}})$ and the pole is $(R_{\text{TOP}} + R_{\text{BOT}}) / (R_{\text{TOP}} \times R_{\text{BOT}} \times C_{\text{SPD}})$. At low frequency level below zero $V_{\text{OUT}}$ will be multiplication of $R_{\text{BOT}} / (R_{\text{TOP}} + R_{\text{BOT}})$ which means feedback by 0.8 / $V_{\text{OUT}}$ and when higher frequency level than the pole it will be feedback by 1.

At VFM mode the ripple of $V_{\text{OUT}}$ is generated by 40 mV (Typ.) higher than that of the reference voltage at PWM mode which is 0.8 V. For all operating frequency range, the ripple of $V_{\text{OUT}}$ is feedback by 1 to the FB pin despite the output voltage settings ripple of $V_{\text{OUT}}$ will follow reference voltage by setting $C_{\text{SPD}}$ large. The bellow shows the example of setting the $C_{\text{SPD}}$ large, where the ripple of $V_{\text{OUT}}$ is feedback by 1 to the FB pin, and setting the $C_{\text{SPD}}$ small, where the ripple of $V_{\text{OUT}}$ is feedback by the multiple of $R_{\text{BOT}} / (R_{\text{TOP}} + R_{\text{BOT}})$.

As shown in the above figure, the ripple of $V_{\text{OUT}}$ becomes larger when the $C_{\text{SPD}}$ is small.

RICOH
The recommended $C_{SPD}$ value is selected to minimize the ripple of $V_{OUT}$. When changing the $R_{BOT}$ value from the recommended value, please make sure the $R_{BOT} \times C_{SPD}$ is also in the range of the recommended value and change the $C_{SPD}$ together. Also, changing $L$, $C_{OUT}$, $R_{ER}$, $C_{EC}$ from the recommended value is required to change the $C_{SPD}$.

Furthermore, if the ripple of the $V_{OUT}$ is permissible, improving the loop stability is possible by adjusting the positive bump of the zero and pole. First, measure the voltage drop of the output by the load transient response without $C_{SPD}$. Then measure the voltage drop again with attachment of small enough $C_{SPD}$. If the selected $C_{SPD}$ is too small, the amount of the voltage drop will be the same value as the value without $C_{SPD}$. Repeat the procedure with increasing $C_{SPD}$ value gradually. When the voltage drop begins to improve, suppose that value as $C_{SPD1}$. Further try other $C_{SPD}$ value by increasing it gradually, then the voltage drop improvement will stop. Suppose that the $C_{SPD}$ value as $C_{spd2}$. The appropriate $C_{SPD}$ value can be calculated as the next formula; $C_{SPD} = \sqrt{(C_{SPD1} \times C_{SPD2})}$. The zero will be low and pole will be high of the feedback resistor at the whole frequency range, the ripple at FVM mode will be lower than that $V_{OUT}$ ($C_{SPD}$ small) of above diagram.

**FLAG Output Function**

The R1270S has an Nch open drain FLAG output. When abnormality is detected, the R1270S switches the Nch transistor On, and sets the FLG pin to “Low”. When the abnormality is removed, the R1270S switches the Nch transistor Off and sets the FLG pin to “High” ($V_{FLGIN}$). The UVD will function only when $V_{FB} < 0.64$ V (Typ.) and at max duty detection or $V_{FB} < 0.64$ V (Typ.) and current limit detection to prevent abnormal output behavior at load transient and input transient response. The following are the abnormal conditions that the IC can detect.

- CE = “L” (Shut down)
- UVLO (Shut down)
- Thermal Shutdown
- during soft-start time ($C_{ss} < 0.72$ V)
- $V_{FB}$ Under Voltage Detection (Typ.0.64 V) and maxduty detection
- $V_{FB}$ Under Voltage Detection (Typ.0.64 V) and current limit detection
- LMT pin Over Voltage Protection (Typ.1.2 V)
- Absolute maximum 6V pin (except FB pin, LMT pin, EC pin) Over Voltage Detection (Typ. 3.0 V)
- When the latch protection runs (R1270S001A)

The FLG pin is designed to keep 0.4 V or less when the current running into the FLG pin is at 1 mA. The recommended values of $V_{FLGIN}$ and $R_{FLG}$ are 6 V or less for $V_{FLGIN}$ and 10 kΩ to 100 kΩ for $R_{FLG}$. When the FLAG function is not used, set the FLG pin OPEN or connect to GND.
"H" is detected under abnormal condition.

R1270S001A/B FLAG Circuit

- $V_{CE}$: 1.0 V
- $V_{FB}$: 0.800 V (Typ.), $V_{UVD}$: 0.64 V (Typ.), 0.72 V (Typ.)
- $V_{FLG}$: 0.4 V >
- $V_{FLGIN}$: Time
- $t_{ss}$: Time

R1270S001A/B FLG Start-up / Shut-down Sequence
Soft-Start Time Function

The soft-start time is between from "H" level of CE to 90% of FB (0.72 V). The soft-start time for the R1270S could be adjusted by using an external capacitor \( C_{SS} \) at the SS pin from minimum of internal soft-start time typical 0.4 ms. The charging current of the external \( C_{SS} \) is 2.0 \( \mu \)A (Typ.) and the soft-start time becomes 3.6 ms typically (reaching the set output voltage is 4.0 ms (Typ.)) when \( C_{SS} \) is 0.01 \( \mu \)F. If not required to adjust the soft-start time, set the SS pin OPEN. On the condition described in the chapter of "Electrical Characteristics", the R1270S guarantees each of soft-start time (\( t_{ss1}/t_{ss2} \)) when the SS pin is set to “Open” or when \( C_{SS} \) is set to 0.01 \( \mu \)F.

![Diagram of soft-start time function](image)

\[
C_{SS} \, \text{[\( \mu \)F]} = 2 \times t_{ss} / 0.72
\]

R1270S001A/B Capacitor for Soft-Start Time Adjustment (\( C_{SS} \)) vs. Soft-Start Time (\( t_{ss} \))

Also, when \( C_{SPD} \) is set large, the rising speed of VOUT may become slower than the soft-start time because of the bypass characteristic of the feedback resistor. Because the R1270S watches the output voltage using the FB pin voltage, the flag detection may be released before the VOUT is fully at set value.

![Diagram of start-up/shutdown sequence](image)

R1270S001A/B Start-up / Shutdown Sequence
**Lx Current Limit**

By using external resistor $R_{LMT}$ to the LMT pin, Lx current limit ($I_{LIMLXH}$), which is high-side switch current limit, can be adjusted as typical 4.5 A at maximum. When $R_{LMT}$ is 54 k$\Omega$, the Lx current limit is set at 2.0 A typical. If not required to adjust Lx current limit, set LMT pin OPEN so that the Lx current limit will be set at typically 4.5 A. Setting at 1.5 A or less is not recommended. On the condition described in the chapter of “Electrical Characteristics”, the R1270S guarantees each of LX limited current ($I_{LIMLXH1}$/$I_{LIMLXH2}$) when connected each of 39 k$\Omega$/220 k$\Omega$ resistors to the LMT pin.

$$R_{LMT} [k\Omega] = \frac{(1200 \times (I_{LIMLXH} \times 0.1033 + 0.13) - 120)}{(12 - 20 \times (I_{LIMLXH} \times 0.1033 + 0.13))}$$

**BST Auxiliary Charge Circuit**

Under the oscillation frequency or conditions of input/output voltage level and load current, the BST capacitor charge may not be sufficient, and hence BST-Lx pin voltage level (Typ. 5.0 V) may not be reached. However, if the output voltage or another power line at 4.5 V to 6.0 V is supplied to the R1270S, a drop of BST pin voltage level can be prevent by connecting BST auxiliary charge circuit with BST pin via a diode. In this case, the voltage of Lx pin must be less than the voltage of the auxiliary charge circuit to charge $C_{BST}$. Also, make sure not to exceed the maximum rating of 6.0 V for BST-Lx. When selecting the diode, 10 mA current rating is more than enough, but also be aware of the voltage rating, and the characteristic of reverse bias leak current at high temperature.
Sequence Composition

By using the soft-start time and the FLAG function (R1270S001A/B), a power up sequence can be composed. The following describes an example application circuit to start up both DC/DC1 and DC/DC2 in a sequence so that the 5.0 V output will not become lower than the DC/DC2 output 3.3 V under the following conditions: the input voltage is 12 V, two lines of output voltages are 5.0 V (DC/DC1) and 3.3 V (DC/DC2), the capacitor of the 5.0 V output is an electrolytic 470 µF, and the capacitor of the 3.3 V output is electrolytic 100 µF.

- **Soft-start time and charging current**
  During the soft-start, the R1270S occurs the charging current ICHRG for the capacitor of VOUT besides the output current IOUT. Therefore, the output current IOUTSS will be given by the following equation,

  \[ I_{OUTSS} = I_{OUT} + I_{CHRG} = I_{OUT} + V_{OUT} \times (C_{OUT} + C_L) / t_{SS} \]

  For the output current on the example application circuit,

  \( (DCDC1) \ I_{OUTSS} = I_{OUT} + V_{OUT} / (C_{OUT} + C_L) / t_{SS} = I_{OUT} + 5.0 \text{ V} \times (10 \mu\text{F} + 470 \mu\text{F}) / 26 \text{ ms} = I_{OUT} + 92 \text{ mA} \)

  \( (DCDC2) \ I_{OUT2SS} = I_{OUT2} + V_{OUT2} / (C_{OUT2} + C_{L2}) / t_{SS} = I_{OUT} + 3.3 \text{ V} \times (10 \mu\text{F} + 100 \mu\text{F}) / 2.6 \text{ ms} = I_{OUT2} + 140 \text{ mA} \)

  Make sure that the output current does not exceed 3.0 A even at soft-start.

- **Using the output of R1270S as the flag pull-up voltage**
  The R1270S has an Nch open drain FLAG output. When detecting an abnormal condition, the R1270S switches the Nch transistor On and sets the FLG pin to “Low”. If the detected condition is not applicable under the FLAG output function, FLAG output will reset to “High” after the completion of the soft-start. When using the VOUT as the VFLGIN, “High” level of the VFLG becomes the same with VOUT.

- **Using the FLAG output as CE pin input for another R1270S**
  The minimum VCEL is 0.85 V and the maximum VCEH is 1.15 V. The maximum VFLGL is 0.4 V, and VFLGH for DC/DC1 on the example circuit is 5.0 V. So, VFLG is usable as CE input for DC/DC2.

- **Using the FLAG output as auto-discharge function**
  When being shut down, the R1270S switches the Nch transistor On and sets the FLG pin to “Low”. And, VFLGIN sends the FLAG current IFLG via RFLG and Nch transistor. Thereby, the capacitor connected to VOUT can be discharged by using VOUT as VFLGIN.
  The maximum IFLG is that of VFLGIN divided by RFLG. Set RFLG so that maximum IFLG becomes lower than 5 mA. Do not connect VOUT directly to FLG pin because the IFLG may become excessive and may damage the IC. The VFLGL is regulated as IFLG = 1 mA. When the RFLG is set higher than IFLG = 1 mA, the maximum voltage 0.4 V of VFLGL is not guaranteed, hence the FLAG function itself may be spoiled.
(DCDC1) R1270S001A/B: $V_{IN} = 12\, V$, $V_{OUT} = 5.0\, V$, $t_{ss} = 40\, ms$ ($C_{SS} = 0.1\, \mu F$)

(DCDC2) R1270S001A/B: $V_{IN} = 12\, V$, $V_{OUT} = 3.3\, V$, $t_{ss} = 4.0\, ms$ ($C_{SS} = 0.01\, \mu F$)
Operation of Buck Converter and Output Current

The DC/DC converter charges energy in the inductor when the switch turns on, and discharges the energy from the inductor when the switch turns off and controls with less energy loss, so that a lower output voltage than the input voltage is obtained. Refer to the following figures.

**Basic Circuit**

Step 1: The switch turns on and current \(i_1\) flows, and energy is charged into \(C_{OUT}\). At this moment, \(IL\) increases from \(IL_{min} (=0)\) to reach \(IL_{max}\) in proportion to the on-time period (ton) of the switch.

Step 2: When the switch turns off, the diode turns on in order to maintain \(IL\) at \(IL_{max}\), and current \(i_2\) flows.

Step 3: \(IL\) \((=i_2)\) decreases gradually and reaches \(IL = IL_{min} = 0\) after a time period of topen, and the diode turns off. This case is called as discontinuous mode. If the output current becomes large, next switching cycle starts before \(IL\) becomes 0 and the diode turns off. In this case, \(IL\) value increases from \(IL_{min} (>0)\), and this case is called continuous mode.

As for the PWM control system, the output voltage is maintained by controlling the on-time period (ton), with the oscillator frequency (fosc) being maintained constant.
Output Current and Selection of External Components

The relation between the output current and external components is as follows:

When the switch of Lx turns on:
(Wherein, the peak to peak value of the ripple current is described as $I_{RP}$, the ON resistance of the switch is described as $R_{ONH}$, and the diode forward voltage as $V_F$, and the DC resistance of the inductor is described as $R_L$, and on time of the switch is described as $t_{on}$)

$$V_{IN} = V_{OUT} + (R_{ONH} + R_L) \times I_{OUT} + L \times I_{RP} / t_{on}$$  \hspace{1cm} \text{Equation 1}

When the switch turns off (the diode turns on) as $t_{off}$:

$$L \times I_{RP} / t_{off} = V_F + V_{OUT} + R_L \times I_{OUT}$$  \hspace{1cm} \text{Equation 2}

Put Equation 2 to Equation 1 and solve for ON duty of the switch, $t_{on} / (t_{on} + t_{off}) = D_{ON}$,

$$D_{ON} = (V_{OUT} + V_F + R_L \times I_{OUT}) / (V_{IN} + V_F - R_{ONH} \times I_{OUT})$$ \hspace{1cm} \text{Equation 3}

Ripple Current is as follows:

$$I_{RP} = (V_{IN} - V_{OUT} - R_{ONH} \times I_{OUT} - R_L \times I_{OUT}) \times D_{ON} / f_{osc} / L$$ \hspace{1cm} \text{Equation 4}

Then, peak current that flows through L, and the peak current $I_{L\text{max}}$ is as follows:

$$I_{L\text{max}} = I_{OUT} + I_{RP} / 2$$ \hspace{1cm} \text{Equation 5}

As for the valley current $I_{L\text{min}}$,

$$I_{L\text{min}} = I_{OUT} - I_{RP} / 2$$ \hspace{1cm} \text{Equation 6}

If $I_{L\text{min}} < 0$, the step-down DC/DC converter operation becomes current discontinuous mode. Therefore the current condition of the current discontinuous mode, the next formula is true.

$$I_{OUT} < I_{RP} / 2$$ \hspace{1cm} \text{Equation 7}

Consider $I_{L\text{max}}$ and $I_{L\text{min}}$, conditions of input and output and select external components.

*The above explanation is based on the calculation in an ideal case in continuous mode.
Ripple Current and Lx Limited Current
The ripple current of the inductor may change according to the various reasons. In the R1270S series, as an Lx current limit, Lx peak current limit is used. Therefore the upper limit of the inductor current is fixed.
The peak current limit is not the average current of the inductor (output current). If the ripple current is large, peak current becomes also large. The characteristic is used for the fold back current limit of version B/D. In other words, the peak current limit is maintained and the switching frequency is reduced, as a result, the average current of the inductor is reduced. To release this condition, the peak current must not exceed the peak current limit.

Latch Protection Function (R1270S001A)
The latch function is enabled after the completion of the soft-start. The latch function works after detecting current limit and starts the internal counter. After the internal counter reaches 2 ms (Typ.), the latch function turns the output off. The R1270S has two ways to reset the latch function: one is to set the CE pin “L”, and another one is to set the VIN voltage to become equal to the detection voltage of the UVLO function, or become less. Also, the latch function is reset when the FB pin voltage is 2.0 V (Typ.) or more.
The start condition for the internal counter is to detect the limited current at each clock, and the reset condition is when a frame without detecting the limit current occurs.
When a ringing between the output voltage and the short-circuit impedance including large inductance occurs and the FB pin voltage exceeds 0.80 V (Typ.), take note that the latch timer might be reset.

Fold-back Protection Function
After the soft-start period, fold back protection is enabled. When there is abnormality to the output and the FB voltage becomes lower than 0.64 V typical, the oscillation frequency will be limited at 1/2. Furthermore, when the output voltage drops below 50% typical from the set voltage (FB pin voltage 0.4 V), oscillation frequency will be limited proportional to the FB pin voltage level.
By reducing frequency, the ripple current increases. The R1270S has the peak current limit function, therefore as in the equation 8, the Lx average current decreases by the increase of the ripple current.

\[ I_{OUT} = I_{Lmax} + \frac{I_{RP}}{2} \]  

Equation 8

If the FB pin voltage becomes less than 0.64 V, the oscillator frequency is reduced to 1/2. At heavy load, if the R1270S becomes into the fold-back protection mode, the situation may not be released by the increased ripple current.
This fold-back protection function is to provide a high degree of safety to the R1270S, not to secure reliability. When using the IC without the latch protection function (R1270S001B), a measure to prevent shorting is required.
**Lx Limited Current Function Sequence**
Loss and Efficiency

Illustrated Description for Loss

\[ P_{ON} = R_{ONH} \times I_{OUT}^2 \times \text{On}
duty \quad : \text{loss at switching ON} \]
\[ P_F = \frac{(t_R + t_F)}{2} \times V_IN \times I_{OUT} \times fosc \quad : \text{switching loss} \]
\[ P_{OFF} = V_F \times I_{OUT} \times \text{Off duty} \quad : \text{loss of diode} \]
\[ P_L = R_L \times I_{OUT}^2 \quad : \text{loss of inductor} \]
\[ P_D = V_IN \times I_{SS} \quad : \text{consumption current if IC} \]
\[ P_{PP} = \frac{1}{4} \times R_C \times I_{RP}^2 \quad : \text{loss by ripple of the inductor current} \]

Efficiency \( \eta = \frac{(V_{OUT} \times I_{OUT})}{(V_{OUT} \times I_{OUT}) + P_{ON} + P_F + P_CL + P_D + P_{PP}} \times 100\% \)

The loss that generated by R1270S is \( P_{ON}, P_F, P_D \). These losses are converted to heat inside the IC. Therefore, the R1270S must be used within the condition below is required.

\[ T_j = \theta_{ja} \times (P_{ON} + P_F + P_D) + T_a < 125^\circ C \]
* PLLREF pin must not be “OPEN”. When using the Ricoh’s evaluation board, a pull-down resistor (RPLLREF2: 100kΩ) is contained on the evaluation board.

R1270S001A/B Typical Application Circuit

* When not connecting a phase compensation resistor of RER (the ER pin is “OPEN”), characteristics of load transient response becomes deteriorated, as compared with when connecting the RER resistor. Please make through evaluation before determining whether connecting the RER resister or not.

R1270S001A/B Minimum Composition Circuit
### R1270S001A/B, C<sub>In</sub>, C<sub>Out</sub> Recommended Components

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<th>VIN, VOUT</th>
<th>Capacitor (µF)</th>
<th>Spec.</th>
<th>Component Name</th>
<th>Maker</th>
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<td>0.47</td>
<td>25 V/125°C</td>
<td>CGA4J2X7R1E474K</td>
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</tr>
<tr>
<td>≤ 16 V</td>
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<td>25 V/125°C</td>
<td>CGA4J3X7R1E225K</td>
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<tr>
<td>All</td>
<td>2.2</td>
<td>50 V/125°C</td>
<td>CGA5L3X7R1H225K</td>
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</tbody>
</table>

### R1270S001A/B, C<sub>Bst</sub> Recommended Components

<table>
<thead>
<tr>
<th>VOUT</th>
<th>Capacitor (µF)</th>
<th>Spec.</th>
<th>Component Name</th>
<th>Maker</th>
</tr>
</thead>
<tbody>
<tr>
<td>All</td>
<td>0.47</td>
<td>16 V</td>
<td>EMK212BJ474KD-T</td>
<td>Taiyo Yuden</td>
</tr>
<tr>
<td>All</td>
<td>0.47</td>
<td>25 V</td>
<td>CGA4J2X7R1E474K</td>
<td>TDK</td>
</tr>
</tbody>
</table>

### R1270S001A/B, D Recommended Components

<table>
<thead>
<tr>
<th>VIN</th>
<th>Spec.</th>
<th>Component Name</th>
<th>Maker</th>
</tr>
</thead>
<tbody>
<tr>
<td>All</td>
<td>40 V/3 A</td>
<td>RB056L-40TE</td>
<td>ROHM</td>
</tr>
<tr>
<td>All</td>
<td>40 V/3 A</td>
<td>RB058L-40TE</td>
<td></td>
</tr>
<tr>
<td>All</td>
<td>60 V/3 A</td>
<td>RB058L-60TE</td>
<td></td>
</tr>
<tr>
<td>All</td>
<td>40 V/3 A</td>
<td>CMS30I40A</td>
<td>TOSHIBA</td>
</tr>
</tbody>
</table>

### R1270S001A/B, L Recommended Components

<table>
<thead>
<tr>
<th>Inductor</th>
<th>Spec.</th>
<th>Component Name</th>
<th>Maker</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.0 µH</td>
<td>6.4 A</td>
<td>RLF7030T-1R0N6R4</td>
<td></td>
</tr>
<tr>
<td></td>
<td>6.5 A</td>
<td>CLF7045NIT-1R0N-D</td>
<td></td>
</tr>
<tr>
<td>1.5 µH</td>
<td>7.3 A</td>
<td>CLF7045T-1R5-D</td>
<td></td>
</tr>
<tr>
<td></td>
<td>5.4 A</td>
<td>CLF7045NIT-1R5N-D</td>
<td></td>
</tr>
<tr>
<td>2.2 µH</td>
<td>5.5 A</td>
<td>CLF7045T-2R2-D</td>
<td></td>
</tr>
<tr>
<td></td>
<td>5.1 A</td>
<td>CLF7045NIT-2R2N-D</td>
<td></td>
</tr>
<tr>
<td>4.7 µH</td>
<td>5.4 A</td>
<td>CLF100040T-4R7-D</td>
<td>TDK</td>
</tr>
<tr>
<td></td>
<td>4.1 A</td>
<td>CLF10060NIT-4R7N-D</td>
<td></td>
</tr>
<tr>
<td>10 µH</td>
<td>4.0 A</td>
<td>CLF10040T-100M-D</td>
<td></td>
</tr>
<tr>
<td>10 µH</td>
<td>3.0 A</td>
<td>CLF10060NIT-100M-D</td>
<td></td>
</tr>
<tr>
<td>15 µH</td>
<td>6.7 A</td>
<td>CLF12555T-100M-D</td>
<td></td>
</tr>
<tr>
<td></td>
<td>6.4 A</td>
<td>CLF12577NIT-100M-D</td>
<td></td>
</tr>
<tr>
<td>22 µH</td>
<td>5.4 A</td>
<td>CLF12555T-150M-D</td>
<td></td>
</tr>
<tr>
<td></td>
<td>5.1 A</td>
<td>CLF12577NIT-150M-D</td>
<td></td>
</tr>
<tr>
<td></td>
<td>4.2 A</td>
<td>CLF12555T-220M-D</td>
<td></td>
</tr>
<tr>
<td></td>
<td>4.3 A</td>
<td>CLF12577NIT-220M-D</td>
<td></td>
</tr>
</tbody>
</table>
Selection of External Components

- Using ceramic capacitors with low ESR (Equivalent Series Resistance) are recommended. The recommended capacitor for $C_{IN}$ between $VIN$ and $GND$ is 4.7 $\mu$F or more. Verify the bias dependence and the temperature characteristics of the ceramic capacitors. Recommended conditions are written based on the case which the recommended parts are used with the R1270S.

- The R1270S is designed with the recommended inductance value and the $C_{OUT}$ ceramic capacitor value to make phase compensation. If the inductance value is large, a lack of the current sensing amount in the current mode might result in an unstable operation. Oppositely, if the inductance value is small, an excess of the current sensing amount might result in the occurrence of the low frequency oscillation on when the on duty ratio is beyond 50%. Ensure that capacitors using for $C_{OUT}$ can meet the voltage-dependent properties in order to have bias dependence. Recommended conditions are written based on the case which the recommended parts are used with the R1270S.

- If the inductance value is small, a ripple to inductor current will be increased and the peak current of the switching will be increased as the load current increases. As a result, the current might reach the current limit value and the current limit might work.

- As for the diode, connect a schottky diode with small capacitance between terminals. The reference characteristic of the capacitance between terminals is around 100 pF or less at 10 V. If using a schottky diode with large capacitance, the operation of the R1270S might be unstable by a flow of an excess switching current. When the capacitance of the schottky diode used is beyond 100 pF at 10 V or is unknown, make sure that the R1270S does not have issues of the load regulation, the line regulation, and the load transient response. And, connect a diode having the smallest possible reverse current IR. Especially, IR’s rising under high temperature conditions might cause a thermal runaway and will lead to cause damage to the IC.

- Output voltage ($V_{OUT}$) can be set by adjustable values of $R_{TOP}$ and $R_{BOT}$ being expressed by the following equation, $V_{OUT} = V_{FB} \times (R_{TOP} + R_{BOT}) / R_{BOT}$. For example, when setting $V_{OUT} = 12$ V, and setting $R_{BOT} = 16$ k$\Omega$, $R_{TOP} = (12$ V / $0.8$ V-1) $\times$ $16$ k$\Omega$ = 224 k$\Omega$. By using the E24 type resistors to make 224 k$\Omega$, you need $(200$ k$\Omega$ + $24$ k$\Omega$) and use them in series. If the tolerance level of the output voltage is relatively wide you may set the output voltage as 11.80 V = 0.8 V $\times$ (220 k$\Omega$ + 16 k$\Omega$) / 16 k$\Omega$. In this case $R_{TOP}$ will be a single resistor of 220 k$\Omega$. When the values of $R_{TOP}$ and $R_{BOT}$ become larger, the R1270S is susceptible to noise with increasing the impedance of FB pin. The recommended value range of $R_{BOT}$ is approximately between 1.0 k$\Omega$ to 160 k$\Omega$. If the operation is unstable, reduce the impedance of FB pin.
As for the CE pin and the PLLREF pin, an up diode for VIN, which have efficacy as ESD protection element, is internally connected to each pin. If CE pin voltage or PLLREF pin voltage may become higher than VIN pin voltage, connect a resistor between CE or PLLREF and VIN pin to prevent flowing large current from CE pin or PLLREF pin to VIN pin. When using external oscillation synchronization, the input signal must be used to become lower than the VIN voltage without using a resistor because the input voltage of PLLREF is filtered out via the resistor.

When using a phase compensation resistor pin (ER pin), the recommended value range of RER is 220 kΩ or more. If not using phase the compensation resistor pin, the ER pin must be set to “OPEN”.

The BST voltage might fall depending on how to use the R1270S. By drops of the BST voltage, R1270S might not function properly. As result, the current limit detection may be caused by an inductor current lower than the set current limit value by reducing the effect.

The R1270S has the driver buffer and the BST voltage detector between BST and Lx pins. When the R1270S is in PWM fixed mode and the light load current is caused by requiring the consumption current always, VOUT might move up by the consumption current. In this case, the load current including the feedback resistor must be set to 0.5 mA or more. In VFM/PWM alternative mode, the R1270S has no problem, as long as RBOT is set between 1.0 kΩ and 160 kΩ.

Recommended ratings to principal set output voltages are as following:

### R1270S001A/B, 300 kHz Recommended Constant

<table>
<thead>
<tr>
<th></th>
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<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>0.8 ≤ VOUT ≤ 1.5</td>
<td>10</td>
<td>10</td>
<td>47</td>
<td>0.47</td>
<td>Open</td>
<td>*1 160</td>
<td>Open</td>
<td>470</td>
<td>2200</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1.0 ≤ VOUT ≤ 6</td>
<td>10</td>
<td>10</td>
<td>47</td>
<td>0.47</td>
<td>100 [1000]*4</td>
<td>*1 160 [16]*4</td>
<td>Open</td>
<td>470</td>
<td>2200</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1 ≤ VOUT ≤ VIN × DMAX*2</td>
<td>10</td>
<td>15</td>
<td>47</td>
<td>0.47</td>
<td>100 [1000]*4</td>
<td>*1 160 [16]*4</td>
<td>Open</td>
<td>470</td>
<td>2200</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### R1270S001A/B, 1000 kHz Recommended Constant

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>0.8 ≤ VOUT ≤ 1.5</td>
<td>4.7</td>
<td>2.2</td>
<td>47</td>
<td>0.47</td>
<td>Open</td>
<td>*1 16</td>
<td>62</td>
<td>470</td>
<td>220</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1 ≤ VOUT ≤ 6</td>
<td>4.7</td>
<td>2.2</td>
<td>47</td>
<td>0.47</td>
<td>2200</td>
<td>*1 16</td>
<td>62</td>
<td>470</td>
<td>220</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1 ≤ VOUT ≤ 15</td>
<td>4.7</td>
<td>4.7</td>
<td>47</td>
<td>0.47</td>
<td>2200</td>
<td>*1 16</td>
<td>62</td>
<td>470</td>
<td>220</td>
<td></td>
<td></td>
</tr>
<tr>
<td>5 ≤ VOUT ≤ VIN × DMAX</td>
<td>4.7</td>
<td>4.7</td>
<td>47</td>
<td>0.47</td>
<td>470</td>
<td>*1 16</td>
<td>62</td>
<td>680</td>
<td>220</td>
<td></td>
<td></td>
</tr>
<tr>
<td>5 ≤ VOUT ≤ VIN × DMAX*2</td>
<td>4.7</td>
<td>10.0</td>
<td>47</td>
<td>0.47</td>
<td>1000</td>
<td>*1 16</td>
<td>62</td>
<td>680</td>
<td>470</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

*1 RTOP = (VOUT / VFB-1) x (RBOT)
*2 Condition recommended at VIN > 18 V
*4 If RBOT is 16 kΩ, the constant value of CSPD requires ten times as much as when RBOT is 160 kΩ.
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R1270S001A/B, 2400 kHz Recommended Constant

<table>
<thead>
<tr>
<th>$V_{OUT}$</th>
<th>$C_{IN}$ [μF]</th>
<th>$L$ [μH]</th>
<th>$C_{OUT}$ [μF]</th>
<th>$C_{BST}$ [μF]</th>
<th>$C_{SPD}$ [pF]</th>
<th>$R_{TOP}$ [kΩ]</th>
<th>$R_{BOT}$ [kΩ]</th>
<th>$R_{RT}$ [kΩ]</th>
<th>$R_{ER}$ [kΩ]</th>
<th>$C_{EC}$ [pF]</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.8 ≤ $V_{OUT}$ ≤ 1.5</td>
<td>4.7</td>
<td>1.0</td>
<td>10</td>
<td>0.47</td>
<td>Open</td>
<td>&quot;&quot;</td>
<td>16</td>
<td>0.0</td>
<td>470</td>
<td>220</td>
</tr>
<tr>
<td>1 ≤ $V_{OUT}$ ≤ 6</td>
<td>2.2</td>
<td>1.0</td>
<td>22</td>
<td>0.47</td>
<td>1000</td>
<td>&quot;&quot;</td>
<td>16</td>
<td>0.0</td>
<td>470</td>
<td>220</td>
</tr>
<tr>
<td>1 ≤ $V_{OUT}$ ≤ 9</td>
<td>2.2</td>
<td>2.2</td>
<td>22</td>
<td>0.47</td>
<td>1000</td>
<td>&quot;&quot;</td>
<td>16</td>
<td>0.0</td>
<td>470</td>
<td>220</td>
</tr>
<tr>
<td>5 ≤ $V_{OUT}$ ≤ $VIN \times DMAX$</td>
<td>2.2</td>
<td>4.7</td>
<td>22</td>
<td>0.47</td>
<td>1000</td>
<td>&quot;&quot;</td>
<td>16</td>
<td>0.0</td>
<td>680</td>
<td>470</td>
</tr>
</tbody>
</table>

*1 $RTOP = (VOUT / VFB-1) \times (Rbot)$
*2 $4.7 \mu F$ or more recommended at $VOUT < 5 V$

TECHNICAL NOTES

The performance of a power source circuit using this device is highly dependent on a peripheral circuit. A peripheral component or the device mounted on PCB should not exceed its rated voltage, rated current or rated power. When designing a peripheral circuit, please be fully aware of the following points. (Refer to PCB Layout Considerations below.)

- External components must be connected as close as possible to the ICs and make wiring as short as possible. Especially, the capacitor connected in between VIN pin and GND pin must be wiring the shortest. If their impedance is high, internal voltage of the IC may shift by the switching current, and the operating may be unstable. Make the power supply and GND lines sufficient.

- The backside thermal pad of the HSOP-18 package must be connected to GND. To improve the thermal dissipation on multi-layered boards, the thermal must be dissipated to another layer by putting some thermal vias on the thermal pad in the land pattern.

- NC pin must be set to “OPEN”.

- Switching regulator is required some caution. Because, a large current variation occurs by the following different current loops in every switching, and a high-frequency noise occurs by parasitic current.
  - The current loop when the switch is “ON”, Input Capacitor ($C_{IN}$) → Hi-side Switch → Inductor → Output Capacitor ($C_{OUT}$) → $C_{IN}$
  - The current loop when the switch is “OFF”, Rectifier Diode ($D$) → Inductor → $C_{OUT}$ → $D$
  - The current loop via Diode Parasitic Capacitor when the switch is “ON”, $C_{IN}$ → Hi-side Switch → Parasitic Capacitor of $D$ → $C_{IN}$

A large EMI noise source is caused in this loop. Therefore, extreme caution is required. These loops have to design as short as possible, and design not to cross lines in the subsequent load side to $C_{OUT}$ in order to avoid the influence of switching noise.
- The line between the Lx pin and the inductor have to wire as close as possible in order to avoid the parasitic capacitor.

- It is recommended the input capacitor (C_in) and the rectifier diode (D) be placed on the same side with the R1270x chip. If placing the other side through via-hole, noise may increase by a parasitic inductance of via. And, it may have the influence on ringing of the Lx pin voltage.

- The power lines (V_in, GND) have to design as widely as possible in order to avoid the parasitic inductance. And, the C_in have to place as close to between V_in and GND as possible.

- On this evaluation board, the land for the Lx pin is wide to connect with large inductor and diode.

- V_out feedback has to be provided near C_out.

- R_top, R_bot, and C_spd pins have to design as close to the FB pin as possible and to keep a distance from the Lx and the BST pins in order to avoid the influence of noise.
TYPICAL CHARACTERISTICS

Note: Typical Characteristics are intended to be used as reference data; they are not guaranteed.

1) FB Voltage vs. Temperature

2) Oscillation Frequency 0 vs. Temperature

3) Maximum Duty cycle 0 vs. Temperature

4) Oscillation Frequency 1 vs. Temperature

5) Maximum Duty cycle 1 vs. Temperature
6) Oscillation Frequency 2 vs. Temperature

![R1270 Oscillation Frequency 2](image)

7) Maximum Duty cycle 2 vs. Temperature

![R1270 Maximum Duty Cycle 2](image)

8) Soft-start time 1 vs. Temperature

![R1270 Soft-Start Time 1](image)

9) Soft-start time 2 vs. Temperature

![R1270 Soft-Start Time 2](image)

10) Delay time for latch protection vs. Temperature

![R1270x001A Delay Time for Latch Protection](image)
11) High side switch current limit1 vs. Temperature  
12) High side switch current limit2 vs. Temperature

![Graph 11: R1270 Hi-side Switch Current Limit 1 (VIN = 5.0V)]

![Graph 12: R1270 Hi-side Switch Current Limit 2 (VIN = 5.0V)]

13) CE “H” Input voltage vs. Temperature  
14) CE “L” Input voltage vs. Temperature

![Graph 13: R1270 CE“H” Input Voltage (VIN = 12V)]

![Graph 14: R1270 CE“L” Input Voltage (VIN = 12V)]

15) Consumption current 1  
16) Consumption current 2

![Graph 15: R1270 Consumption Current 1 (VIN = 34V)]

![Graph 16: R1270 Consumption Current 2 (VIN = 34V)]
17) UVLO Release voltage vs. Temperature

R1270 UVLO Release Voltage

18) UVLO Threshold voltage vs. Temperature

R1270 UVLO Threshold Voltage

19) Output current vs. Efficiency

\[ V_{\text{OUT}} = 1.8 \text{ V} \]

\[ f_{\text{osc}} = 300\text{kHz} / V_{\text{OUT}} = 1.8\text{V} \quad (Ta = 25^\circ\text{C}) \]

\[ f_{\text{osc}} = 450\text{kHz} / V_{\text{OUT}} = 1.8\text{V} \quad (Ta = 25^\circ\text{C}) \]

\[ V_{\text{OUT}} = 3.3 \text{ V} \]

\[ f_{\text{osc}} = 300\text{kHz} / V_{\text{OUT}} = 3.3\text{V} \quad (Ta = 25^\circ\text{C}) \]

\[ f_{\text{osc}} = 450\text{kHz} / V_{\text{OUT}} = 3.3\text{V} \quad (Ta = 25^\circ\text{C}) \]
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**V\text{OUT} = 3.3\text{ V}**

\[f_{osc} = 1000kHz / \text{VOUT} = 3.3\text{V}\]  
\[(T_a = 25\text{°C})\]

**V\text{OUT} = 5.0\text{ V}**

\[f_{osc} = 300kHz / \text{VOUT} = 5.0\text{V}\]  
\[(T_a = 25\text{°C})\]

\[f_{osc} = 450kHz / \text{VOUT} = 5.0\text{V}\]  
\[(T_a = 25\text{°C})\]

\[f_{osc} = 1000kHz / \text{VOUT} = 5.0\text{V}\]  
\[(T_a = 25\text{°C})\]

\[f_{osc} = 2000kHz / \text{VOUT} = 5.0\text{V}\]  
\[(T_a = 25\text{°C})\]
\( V_{OUT} = 7.0 \) V

\( f_{osc} = 300\text{kHz} / V_{OUT} = 7.0V \)  
\( (Ta = 25^\circ C) \)

\( f_{osc} = 450\text{kHz} / V_{OUT} = 7.0V \)  
\( (Ta = 25^\circ C) \)

\( f_{osc} = 1000\text{kHz} / V_{OUT} = 7.0V \)  
\( (Ta = 25^\circ C) \)

\( f_{osc} = 2000\text{kHz} / V_{OUT} = 7.0V \)  
\( (Ta = 25^\circ C) \)
**V_{OUT} = 12 V**

- **f_{osc} = 300kHz / V_{OUT} = 12V**
  - (T_{a} = 25°C)

- **f_{osc} = 450kHz / V_{OUT} = 12V**
  - (T_{a} = 25°C)

- **f_{osc} = 1000kHz / V_{OUT} = 12V**
  - (T_{a} = 25°C)

- **f_{osc} = 2000kHz / V_{OUT} = 12V**
  - (T_{a} = 25°C)

- **f_{osc} = 2400kHz / V_{OUT} = 12V**
  - (T_{a} = 25°C)
20) Load transient response

\[
f_{osc} = 300 \text{ kHz}
\]

\[
f = 300\text{kHz} \;/\; VOUT = 3.3\text{V} \;/\; VFM<=>PWM
\]

\[
\text{VIN} = 12\text{V} \;/\; 0\text{A <-> 1A}
\]

\[
\text{OUTPUT VOLTAGE}
\]

\[
\text{OUTPUT CURRENT}
\]

\[
f = 300\text{kHz} \;/\; VOUT = 3.3\text{V} \;/\; VFM<=>PWM
\]

\[
\text{VIN} = 12\text{V} \;/\; 1\text{A <-> 3A}
\]

\[
\text{OUTPUT VOLTAGE}
\]

\[
\text{OUTPUT CURRENT}
\]
fosc = 1000 kHz

fosc = 1000kHz / VOUT = 3.3V / VFM <=> PWM
VIN = 12V / IOUT = 0A -> 1A

fosc = 1000kHz / VOUT = 3.3V / VFM <=> PWM
VIN = 12V / IOUT = 1A -> 0A

fosc = 1000kHz / VOUT = 3.3V / VFM <=> PWM
VIN = 12V / IOUT = 3A -> 1A
fosc = 2000 kHz

\[ f_{osc} = 2000\text{kHz} / V_{OUT} = 5.0\text{V} / \text{VFM} \Rightarrow \text{PWM} \]

\[ V_{IN} = 12\text{V} / I_{OUT} = 0\text{A} \rightarrow 1\text{A} \]

\[ 4.9 \quad 5 \quad 5.1 \]

\[ 0 \quad 0.04 \quad 0.08 \quad 0.12 \quad 0.16 \text{ time [ms]} \]

\[ \text{Output Voltage [V]} \]

\[ \text{Output Current [A]} \]

\[ f_{osc} = 2000\text{kHz} / V_{OUT} = 5.0\text{V} / \text{VFM} \Rightarrow \text{PWM} \]

\[ V_{IN} = 12\text{V} / I_{OUT} = 1\text{A} \rightarrow 0\text{A} \]

\[ 5 \quad 5.1 \quad 5.2 \]

\[ 0 \quad 0.1 \quad 0.2 \quad 0.3 \quad 0.4 \text{ time [s]} \]

\[ \text{Output Voltage [V]} \]

\[ \text{Output Current [A]} \]

\[ f_{osc} = 2000\text{kHz} / V_{OUT} = 5.0\text{V} / \text{VFM} \Rightarrow \text{PWM} \]

\[ V_{IN} = 12\text{V} / I_{OUT} = 3\text{A} \rightarrow 1\text{A} \]

\[ 4.75 \quad 5 \quad 5.25 \quad 5.5 \]

\[ 0 \quad 0.02 \quad 0.04 \quad 0.06 \quad 0.08 \text{ time [ms]} \]

\[ \text{Output Voltage [V]} \]

\[ \text{Output Current [A]} \]

\[ f_{osc} = 2000\text{kHz} / V_{OUT} = 5.0\text{V} / \text{VFM} \Rightarrow \text{PWM} \]

\[ V_{IN} = 12\text{V} / I_{OUT} = 3\text{A} \rightarrow 1\text{A} \]

\[ 5 \quad 5.25 \quad 5.5 \]

\[ 0 \quad 0.02 \quad 0.04 \quad 0.06 \quad 0.08 \text{ time [ms]} \]

\[ \text{Output Voltage [V]} \]

\[ \text{Output Current [A]} \]
21) Output current vs. Output voltage

For $f_{osc} = 300$ kHz:

- VIN = 12V
- VOUT = 3.3V

For $f_{osc} = 1000$ kHz:

- VIN = 12V
- VOUT = 3.3V

For $f_{osc} = 2000$ kHz:

- VIN = 12V
- VOUT = 5.0V

(Ta = 25°C)
22) Input transient response

**fosc = 300 kHz**

- $f_{osc} = 300\, \text{kHz}$ / $V_{OUT} = 3.3\, \text{V}$ / VFM $\Leftrightarrow$ PWM
- $V_{IN} = 8\, \text{V} \leftrightarrow 16\, \text{V}$ / $I_{OUT} = 0.1\, \text{A}$

**fosc = 1000 kHz**

- $f_{osc} = 1000\, \text{kHz}$ / $V_{OUT} = 3.3\, \text{V}$ / VFM $\Leftrightarrow$ PWM
- $V_{IN} = 8\, \text{V} \leftrightarrow 16\, \text{V}$ / $I_{OUT} = 0.1\, \text{A}$

**fosc = 2000 kHz**

- $f_{osc} = 2000\, \text{kHz}$ / $V_{OUT} = 5.0\, \text{V}$ / VFM $\Leftrightarrow$ PWM
- $V_{IN} = 8\, \text{V} \leftrightarrow 16\, \text{V}$ / $I_{OUT} = 0.1\, \text{A}$
23) Input voltage vs. Output voltage

\(f_{osc} = 300 \text{ kHz}\)

\(f_{osc} = 1000 \text{ kHz}\)

\(f_{osc} = 2000 \text{ kHz}\)
The power dissipation of the package is dependent on PCB material, layout, and environmental conditions. The following measurement conditions are based on JEDEC STD. 51-7.

**Measurement Conditions**

<table>
<thead>
<tr>
<th>Item</th>
<th>Measurement Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Environment</td>
<td>Mounting on Board (Wind Velocity = 0 m/s)</td>
</tr>
<tr>
<td>Board Material</td>
<td>Glass Cloth Epoxy Plastic (Four-Layer Board)</td>
</tr>
<tr>
<td>Board Dimensions</td>
<td>76.2 mm × 114.3 mm × 0.8 mm</td>
</tr>
<tr>
<td>Copper Ratio</td>
<td>Outer Layer (First Layer): Less than 95% of 50 mm Square</td>
</tr>
<tr>
<td></td>
<td>Inner Layers (Second and Third Layers): Approx. 100% of 50 mm Square</td>
</tr>
<tr>
<td></td>
<td>Outer Layer (Fourth Layer): Approx. 100% of 50 mm Square</td>
</tr>
<tr>
<td>Through-holes</td>
<td>ϕ 0.3 mm × 21 pcs</td>
</tr>
</tbody>
</table>

**Measurement Result** (Ta = 25°C, Tjmax = 125°C)

<table>
<thead>
<tr>
<th>Item</th>
<th>Measurement Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Dissipation</td>
<td>3100 mW</td>
</tr>
<tr>
<td>Thermal Resistance (θja)</td>
<td>θja = 32°C/W</td>
</tr>
<tr>
<td>Thermal Characterization Parameter (ψjt)</td>
<td>ψjt = 8 °C/W</td>
</tr>
</tbody>
</table>

θja: Junction-to-Ambient Thermal Resistance  
ψjt: Junction-to-Top Thermal Characterization Parameter

The above graph shows the power dissipation of the package at Tjmax = 125°C and Tjmax = 150°C. Operating the device in the hatched range might have a negative influence on its lifetime. The total hours of use and the total years of use must be limited as follows:

<table>
<thead>
<tr>
<th>Total Hours of Use</th>
<th>Total Years of Use (4 hours/day)</th>
</tr>
</thead>
<tbody>
<tr>
<td>13,000 hours</td>
<td>9 years</td>
</tr>
</tbody>
</table>
PACKAGE DIMENSIONS

HSOP-18

Ver. A

UNIT: mm

HSOP-18 Package Dimensions
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