LOT ASSURANCE INSPECTION

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LOT ASSURANCE INSPECTION is executed to verify the quality every wafer process fabrication lot.
It is the key to the assured delivery initial reliability.

<For Real-Time Clock ICs>

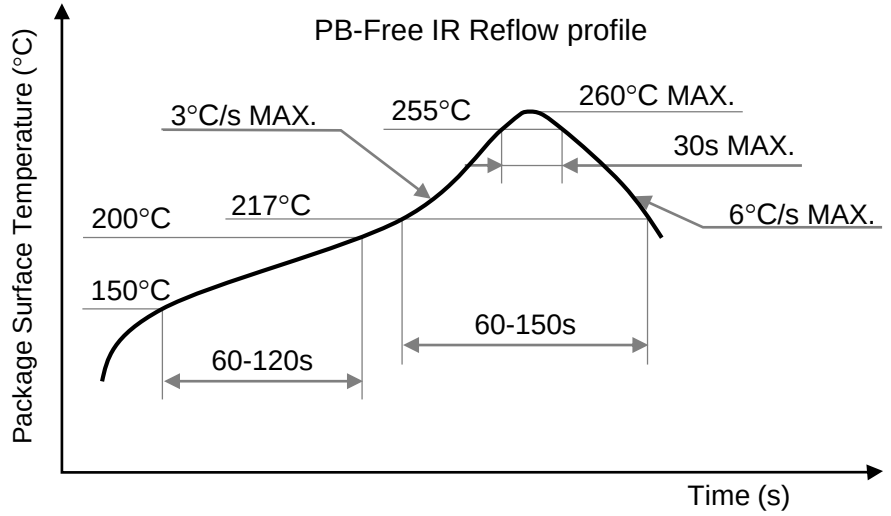
No.	TEST ITEMS	TEST CONDITION	SAMPLE	LTPD
1	High Temperature Operating Life Test	Ta=125°C, 48h	22	10%
2	uHAST	Pre-condition(*) Ta=125°C, RH=85%、20h	22	10%

uHAST: Unbiased Highly Accelerated temperature and humidity Stress Test.

(*)Pre-condition [SMD Package]
Reflow 2times (IR/ Max.260: Following profile.)

< Test Period >

The test period will be change to the periodical monitoring when it is confirmed the good quality level.



QUALITY ASSURANCE TEST INSPECTION

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QUALITY ASSURANCE TEST is done for quality assurance of shipped products by using sampling inspection.

<For Real-Time Clock ICs>

No.	DIVISION	TEST ITEMS	CRITERIA	AQL **
1	Electrical	Major Defect	QAT Specification	0.065% *
		Minor Defect		0.15%
2	Appearance	Major Defect	Visual Inspection Criteria	0.25%
		Minor Defect		0.15%

*) Major Defect (short, open or functionally inoperative) AQL 0.065%

**) AQL : ANSI/ASQC Z1.4-1993

Sampling Plans : Table Ⅱ-C-Single sampling plans for reduced inspection