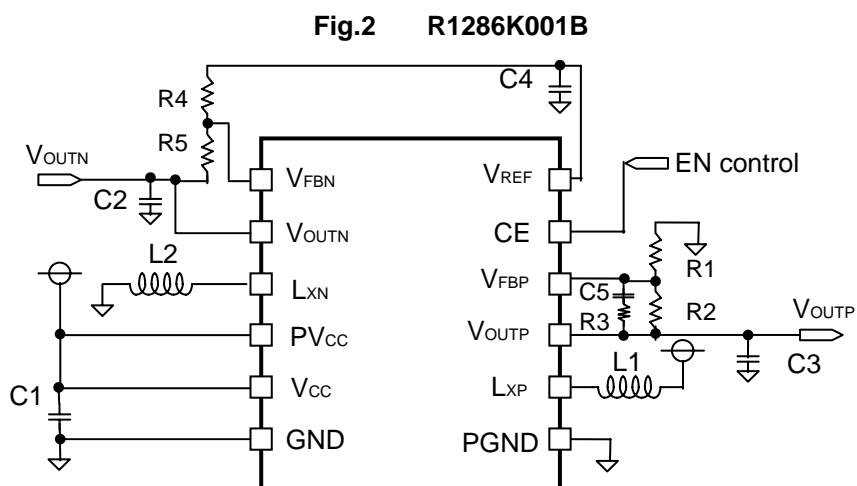
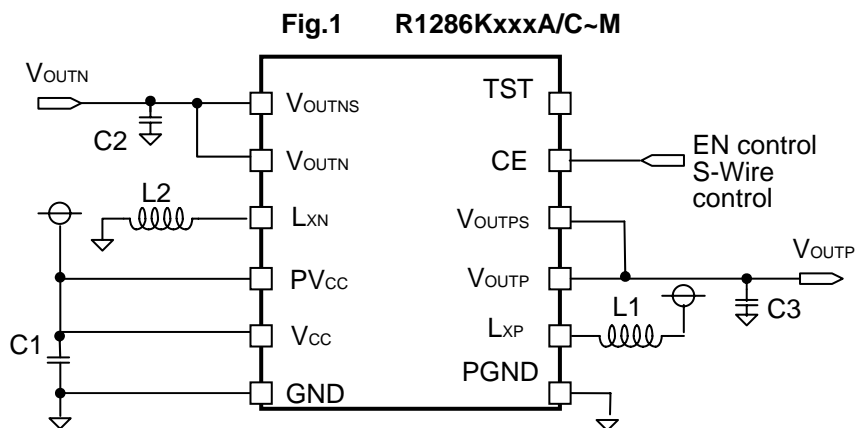


■ TYPICAL APPLICATION



■ RECOMMENDED EXTERNAL COMPONENTS

L1	VLF302510M-4R7M (TDK)
L2	VLF4012S-4R7M (TDK)
C1	C2012X5R0J475K (TDK)
C2	C2012X5R0J475K (TDK)
C3	C2012X5R0J475K (TDK)
C4	0.1 μ F 0603size (001B only)

■ TYPICAL BOARD LAYOUT

● Current Path on PCB

The current paths of boost DC/DC converter are shown in Fig.3 and Fig.4, and the current path of inverting DC/DC converter are shown in Fig.5 and Fig. 6.

The parasitic impedance, inductance, and the capacitance in the parts pointed with red arrows in Fig.4 and Fig.6 have an influence against the stability of the DC/DC converters and become a cause of the noise. Therefore, such parasitic elements must be made as small as possible.

Wiring of the current paths shown in Fig3 to Fig6 must be short and thick.

● Layout Guide for PCB

- Make the wiring of the bypass capacitor (C1) between V_{CC} , PV_{CC} pin and GND pin. The GND pin should be connected to the GND plane of the PCB.

- Place the output capacitors (C1, C2 and C3) as close as possible to the GND pin of the IC.

Notes: To minimize the connection distance, the wiring between GND of C1 and GND of C2 should be running under the IC. Please refer to Board Layout (P.3 Topside).

- The wiring between L_{XP} pin, L_{XN} pin and inductor each should be as short as possible and mount output capacitors (C2 and C3) as close as possible to the V_{OUTP} , V_{OUTN} each.
- Input impedance of V_{OUTPS} pin, V_{OUTNS} pin, V_{FBP} pin, and V_{FBN} pin is high, therefore, the external noise may affect on the performance. The coupling capacitance between these nodes and switching lines must be as short as possible.

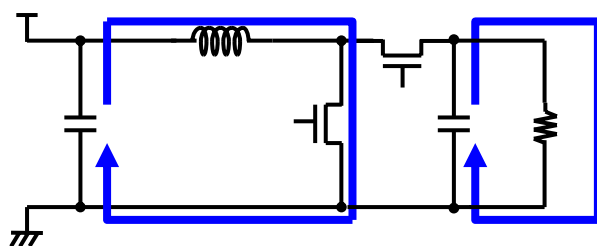


Fig.3 NMOSFET-ON (BOOST)

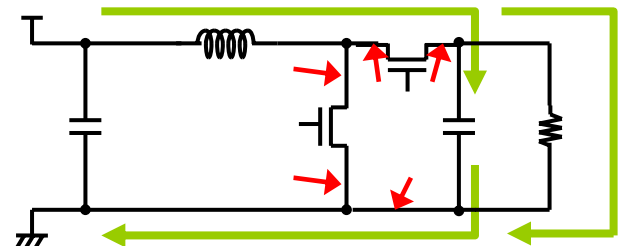


Fig.4 PMOSFET-ON (BOOST)

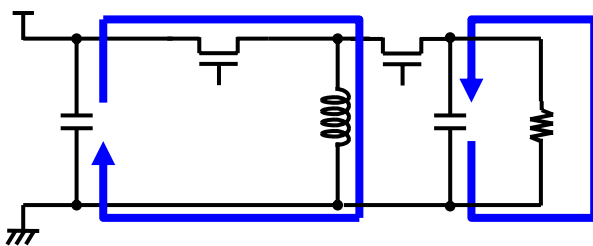


Fig.5 PMOSFET-ON (INVERTING)

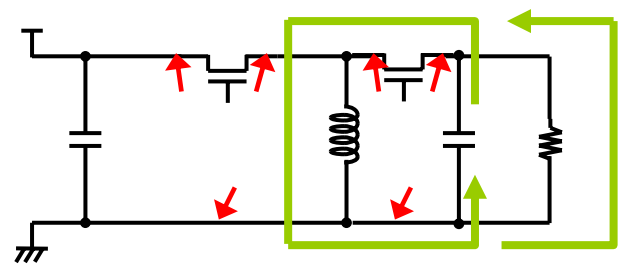
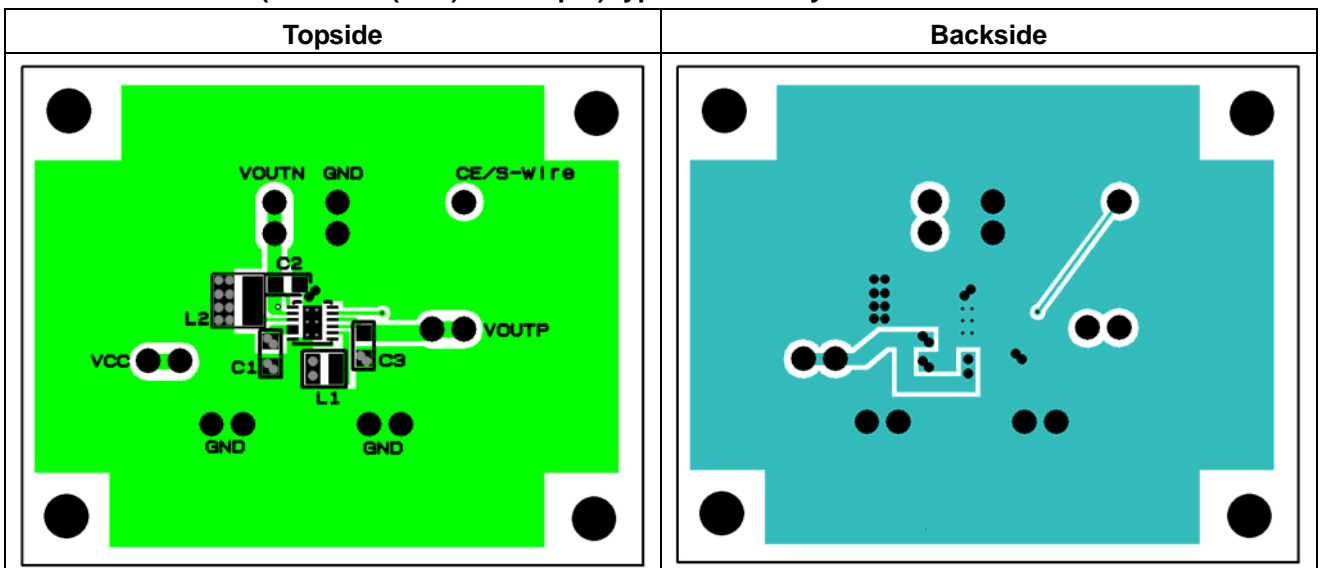


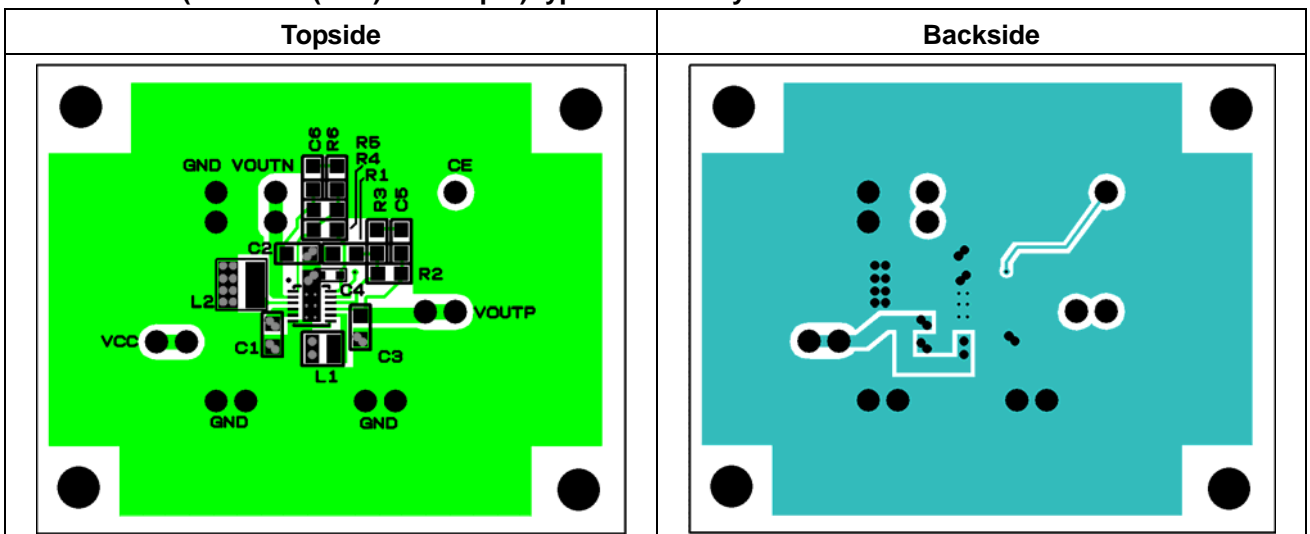
Fig.6 NMOSFET-ON (INVERTING)

● Board Layout

R1286KxxxA/C~N (PKG:DFN(PLP)2730-12pin) typical board layout



R1286K001B (PKG:DFN(PLP)2730-12pin) typical board layout





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