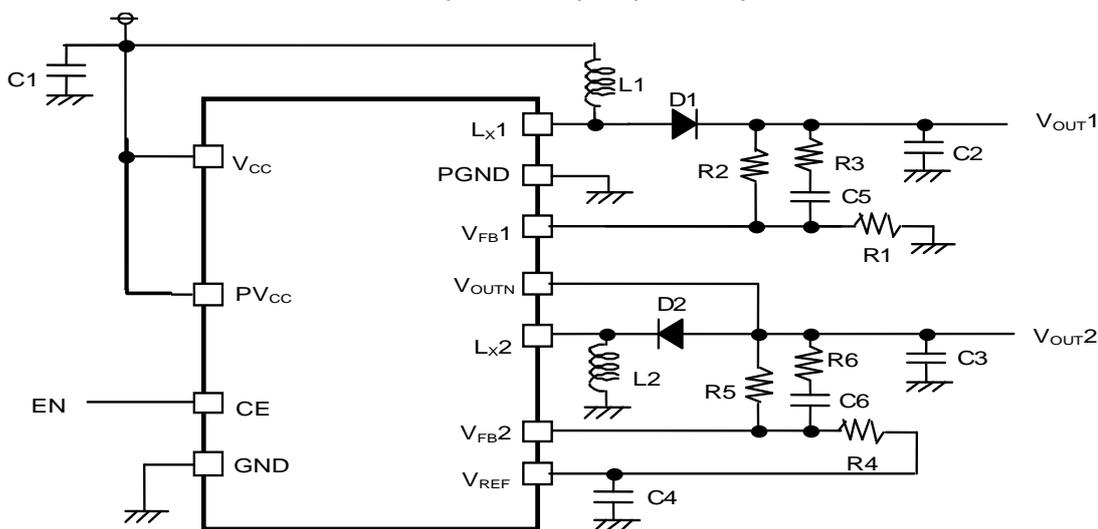


Design Guide

NO.ED-157-150717

■ TYPICAL APPLICATION

R1283K (PKG:DFN(PLP)2730-12)



■ RECOMMENDED EXTERNAL COMPONENTS

● When $V_{out1}=12V$, $V_{out2}=-7.5V$

Symbol	Parts Recommendation		
	R1283x00xA	R1283x00xB	R1283x00xC
L1 / L2	VLF3010A-150M (TDK)	VLF3010ST-6R8M (TDK)	VLF3010ST-4R7M(TDK)
C1	4.7 μ F (6.3V pressure resistance)		
C2	GRM32DB11C106KA01L (Murata) x 2 parallel		
C3	GRM32DB11C106KA01L (Murata)		
C4	0.1 μ F (6.3V pressure resistance)		
D1 / D2	CRS10I30A (TOSHIBA)		

● When $V_{out1}=4.6V$, $V_{out2}=-4.4V$

Symbol	Parts Recommendation		
	R1283x00xA	R1283x00xB	R1283x00xC
L1 / L2	VLF3010A-150M (TDK)	VLF3010ST-4R7M (TDK)	VLF3010ST-4R7M(TDK)
C1	4.7 μ F (6.3V pressure resistance)		
C2	GRM21BB31C106KE15L (Murata)		
C3	GRM21BB31C106KE15L (Murata)		
C4	0.1 μ F (6.3V pressure resistance)		
D1 / D2	CRS10I30A (TOSHIBA)		

■ TYPICAL BOARD LAYOUT

● Current path on PCB

The current paths in an application circuit are shown in Fig.1 and 2(Boost) and Fig.3 and 4(Inverting).

A current flows through the paths shown in Fig.1(Fig.3) at the time of MOSFET-ON, and shown in Fig.2(Fig.4) at the time of MOSFET-OFF.

In the paths pointed with red arrows in Fig.2(Fig.4), current flows just in MOSFET-ON period or just in MOSFET

-OFF period. Parasitic impedance / inductance and the capacitance of these paths influence stability of the system and cause noise outbreak. So please minimize this side effect. In addition, please shorten the wiring of other current paths shown in Fig1 ~ Fig4.

● LAYOUT Guide for PCB

- Externally short V_{CC} pin to PV_{CC} pin. Externally short GND pin to PGND pin.
- Please shorten the wiring of the input capacitor(C1) between V_{CC} , PV_{CC} pin and GND pin of IC. The GND pin should be connected to the strong GND plane.
- The area of L_{X1} and L_{X2} land pattern should be smaller.
- The wiring between L_{X1} and L_{X2} pin and inductor and diode should be short and please put output capacitor (C2 and C3) close to the cathode of diode.
- Please make the GND side of output capacitor(C2 and C3) close to the GND pin of IC.

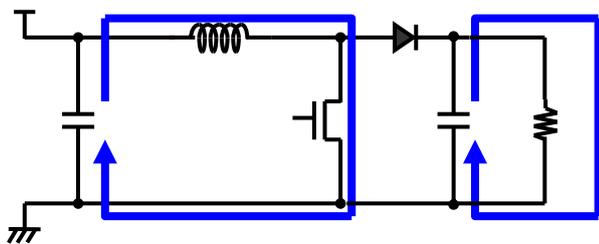


Fig.1 MOSFET-ON(BOOST)

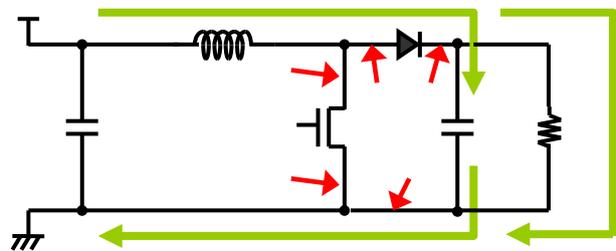


Fig.2 MOSFET-OFF(BOOST)

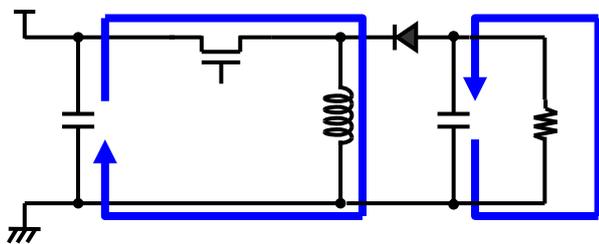


Fig.3 MOSFET-ON(INVERTING)

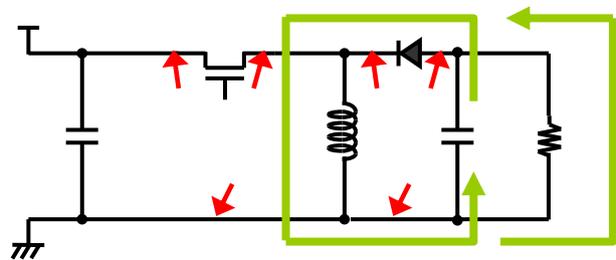
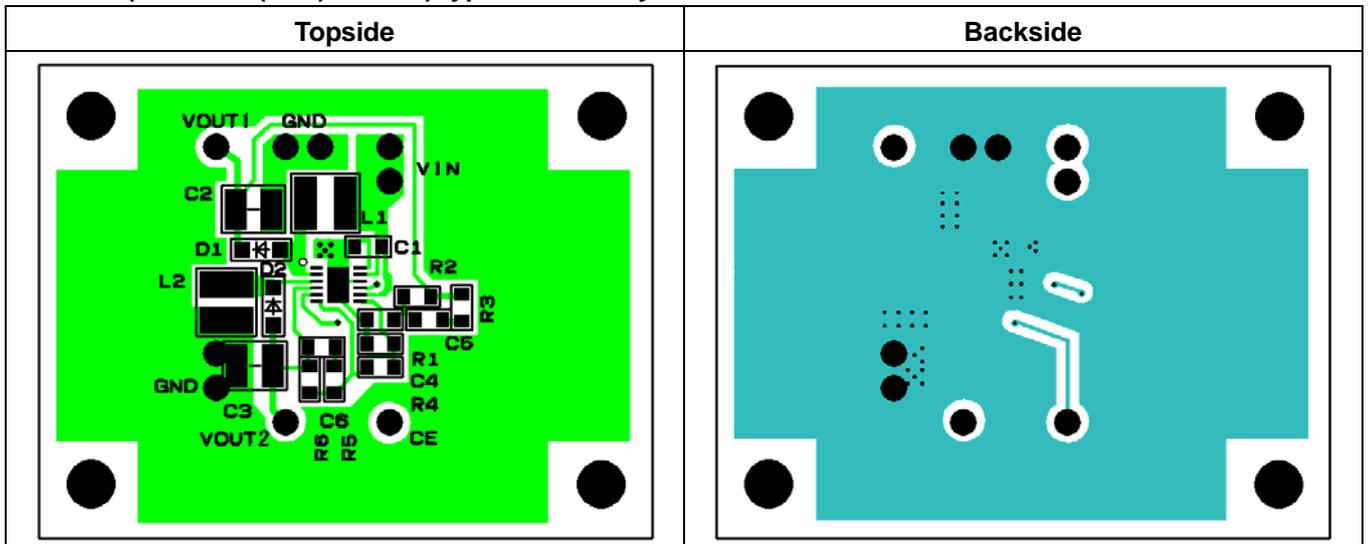


Fig.4 MOSFET-OFF(INVERTING)

●Board Layout

R1283K (PKG:DFN(PLP)2730-12) typical board layout





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