

■ Technical Notes on Layout Pattern

● EMI (Electro-Magnetic Interference) Noise Control

1. Switching regulator is required some caution. Because, a large current variation occurs by the following different current loops in every switching, and a high-frequency noise occurs by parasitic current.

* The current loop when the switch is "ON",

Input Capacitor (C_{IN}) → Hi-side Switch → Inductor → Output Capacitor (C_{OUT}) → C_{IN}

* The current loop when the switch is "OFF",

Rectifier Diode (D) → Inductor → C_{OUT} → D

* The current loop via Diode Parasitic Capacitor when the switch is "ON",

C_{IN} → Hi-side Switch → Parasitic Capacitor of D → C_{IN}

A large EMI noise source is caused in this loop. Therefore, extreme caution is required.

These loops have to design as short as possible, and design not to cross lines in the subsequent load side to C_{OUT} in order to avoid the influence of switching noise.

2. The line between the Lx pin and the inductor have to wire as close as possible in order to avoid the parasitic capacitor.

3. It is recommended the input capacitor (C_{IN}) and the rectifier diode (D) be placed on the same side with the R1270x chip. If placing the other side through via-hole, noise may increase by a parasitic inductance of via. And, it may have the influence on ringing of the Lx pin voltage.

● Control of Malfunction by Voltage Fluctuations

4. The power lines (V_{IN} , GND) have to design as widely as possible in order to avoid the parasitic inductance. And, the C_{IN} have to place as close to between V_{IN} and GND as possible.

Note: On this evaluation board, the land for the Lx pin is wide to connect with large inductor and diode.

5. V_{OUT} feedback has to be provided near C_{OUT} .

● EMS (Electro Magnetic Susceptibility) Improvements

6. R_{TOP} , R_{BOT} , and C_{SPD} pins have to design as close to the FB pin as possible and to keep a distance from the Lx and the BST pins in order to avoid the influence of noise.



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