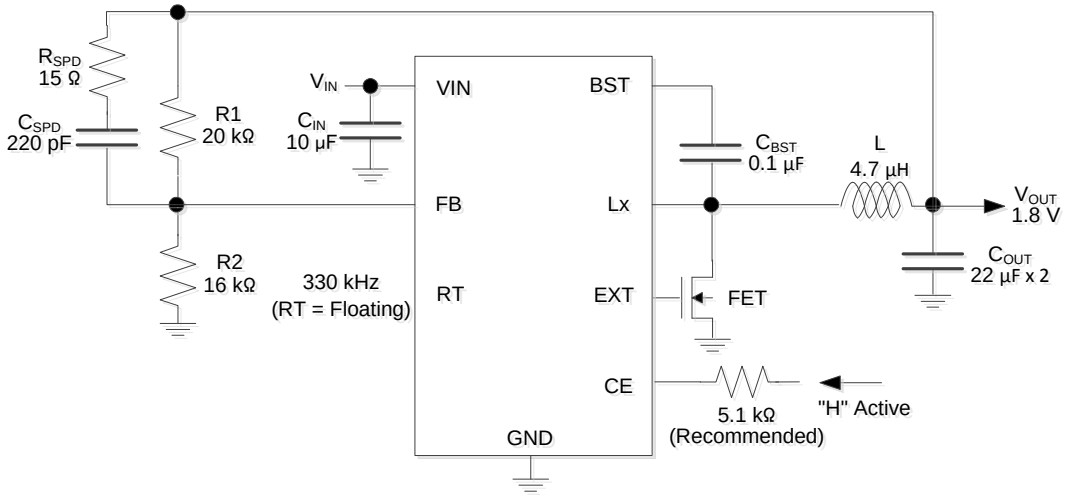
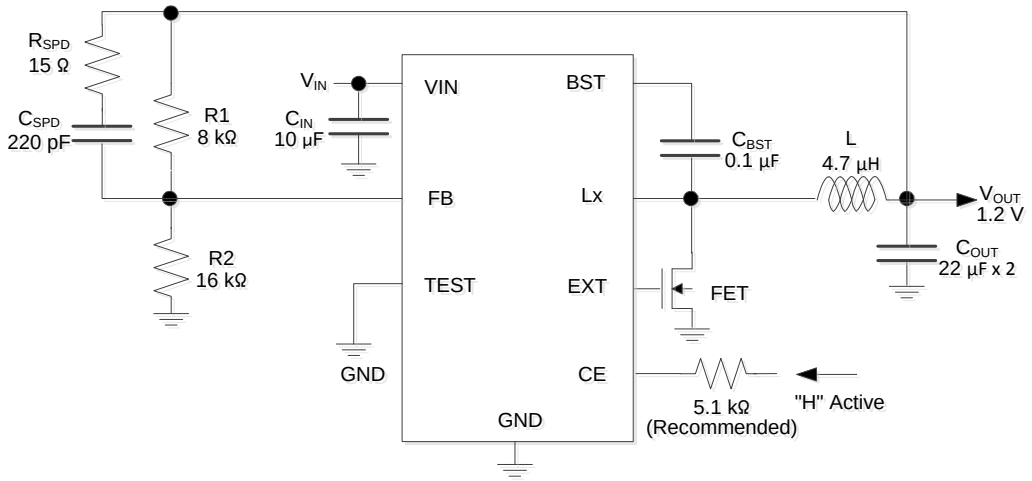
DESIGN GUIDE

NO.ED-191-170327

TYPICAL APPLICATIONS



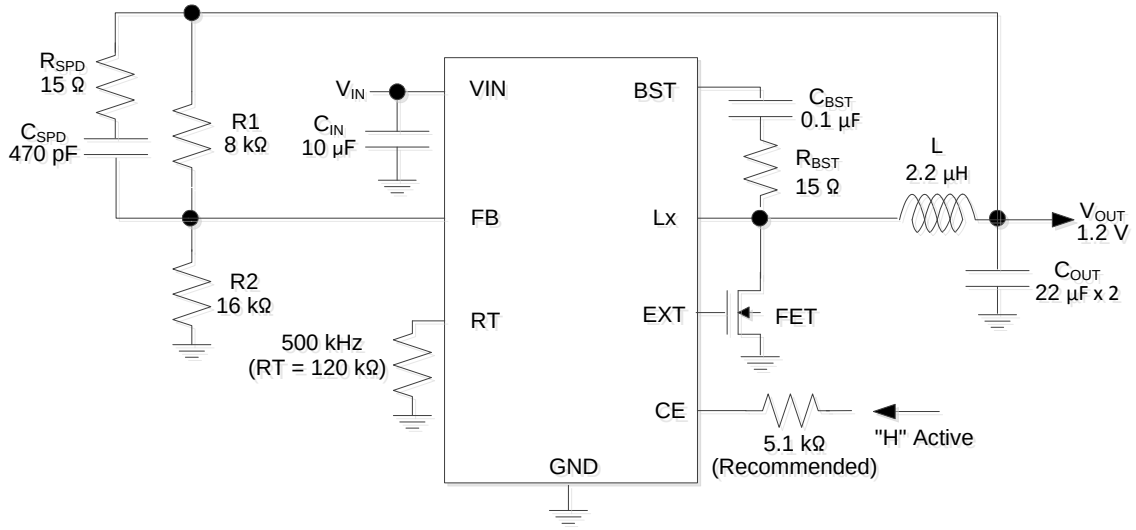
R1242S001A/B Typical Application, V_{OUT} = 1.8 V, 330 kHz



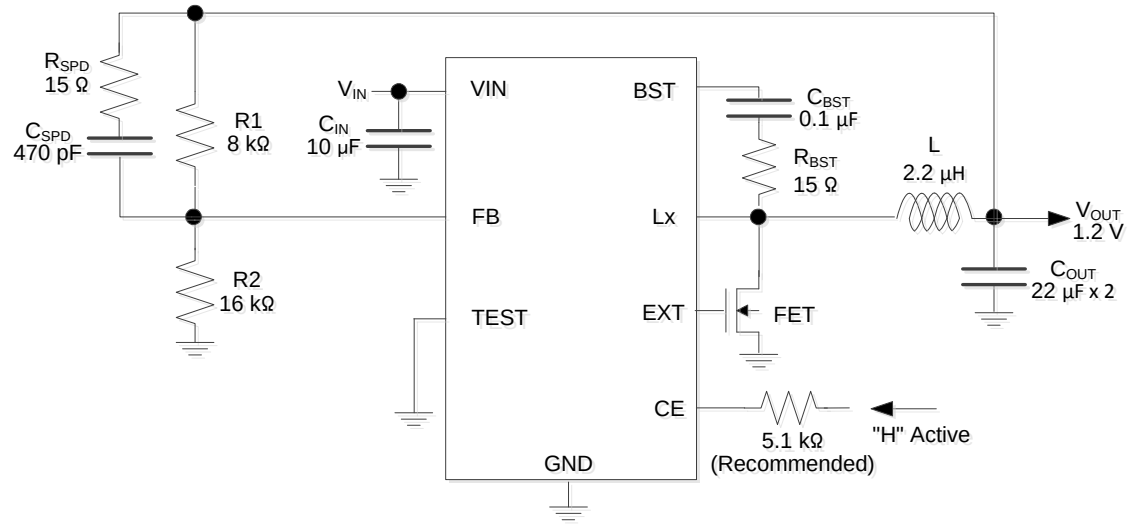
R1242S001C/D Typical Application, V_{OUT} = 1.2 V, 330 kHz

Recommended External Components

C_{IN}	10 µF, UMK325BJ106MM-P (TAIYO YUDEN)
	10 µF, CGA6P3X7S1H106K (TDK)
C_{OUT}	22 µF, GRM31CR71A226M (Murata)
C_{BST}	0.1 µF, GRM21BB11H104KA01L (Murata)
L	4.7 µH, VLF10045T-4R7N6R1 (TDK)
FET	TPN11003NL (TOSHIBA)



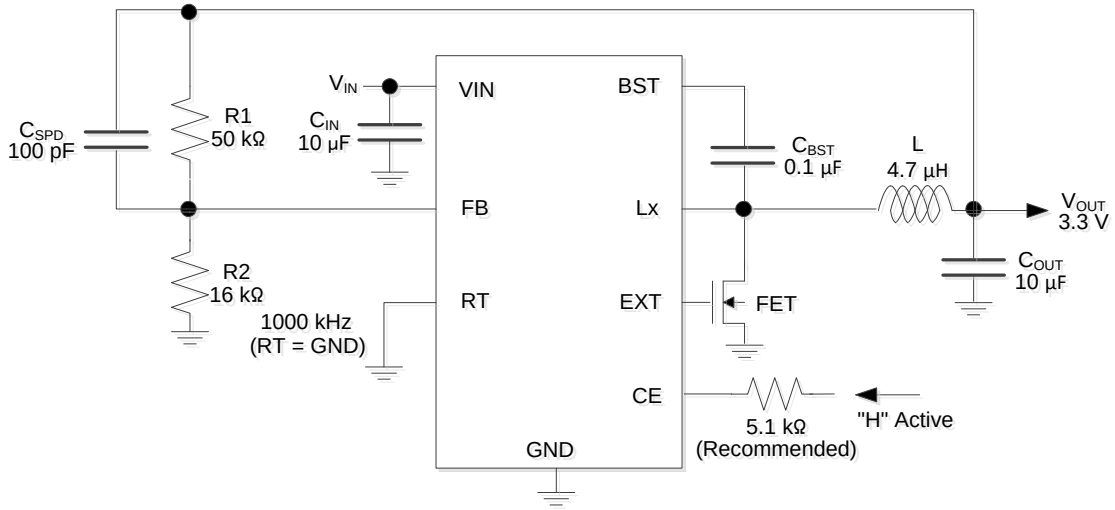
R1242S001A/B Typical Application, V_{OUT} = 1.2 V, 500 kHz



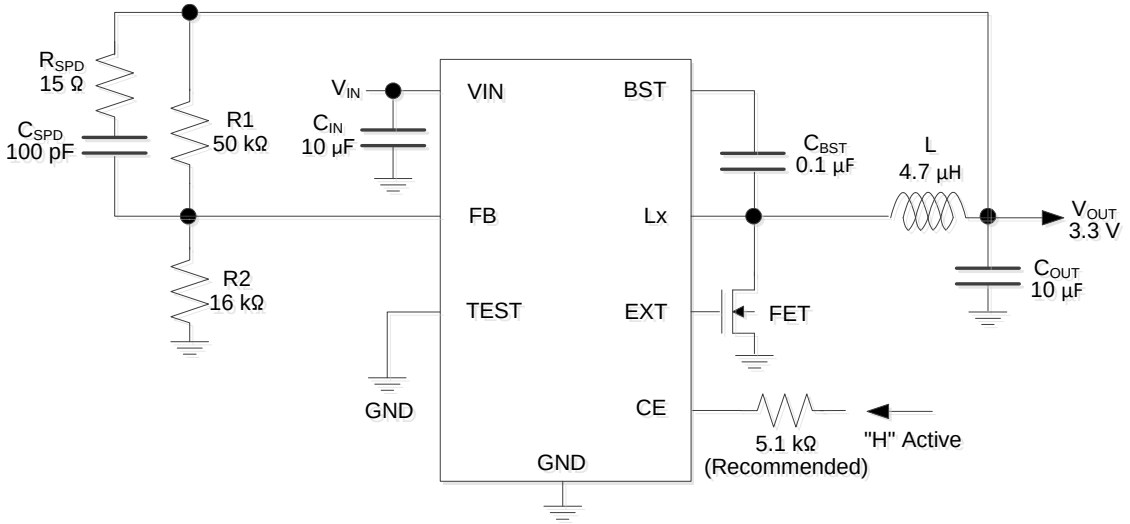
R1242S001E/F Typical Application, V_{OUT} = 1.2 V, 500 kHz

Recommended External Components

C_{IN}	10 µF, UMK325BJ106MM-P (TAIYO YUDEN)
	10 µF, CGA6P3X7S1H106K (TDK)
C_{OUT}	22 µF, GRM31CR71A226M (Murata)
C_{BST}	0.1 µF, GRM21BB11H104KA01L (Murata)
L	2.2 µH, RLF7030T-2R2M5R4 (TDK)
FET	TPN11003NL (TOSHIBA)



R1242S001A/B Typical Application, V_{OUT} = 3.3 V, 1000 kHz



R1242S001G/H Typical Application, V_{OUT} = 3.3 V, 1000 kHz

Recommended External Components

C_{IN}	10 µF, UMK325BJ106MM-P (TAIYO YUDEN)
	10 µF, CGA6P3X7S1H106K (TDK)
C_{OUT}	10 µF, GRM31CR71E106K (Murata)
C_{BST}	0.1 µF, GRM21BB11H104KA01L (Murata)
L	4.7 µH, VLF10045T-4R7N6R1 (TDK)
FET	TPN11003NL (TOSHIBA)

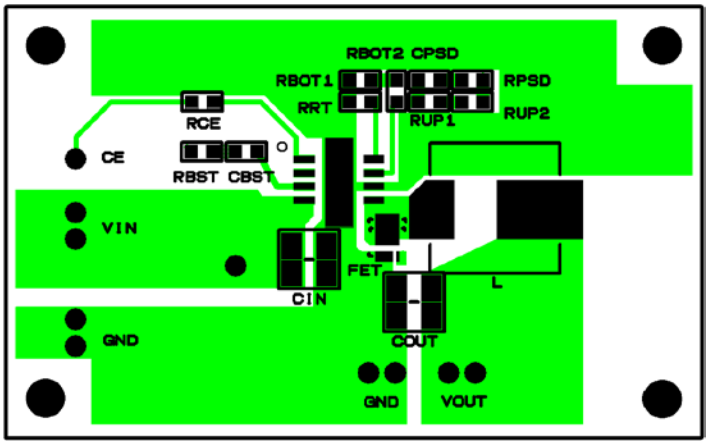
TECHNICAL NOTES ON EXTERNAL COMPONENTS

- External components must be connected as close as possible to the ICs and their wiring must be short as possible. Especially, the capacitor must be connected with the shortest distance between VIN and GND pins. If the impedances of the power supply line and the GND line are high, the operation can be unstable due to the switching current which fluctuates the electric potential of the inside the ICs. The impedances of power supply line and GND line must be as low as possible. When designing their wirings, it is necessary to give careful consideration to the large current flowing into the power supply, GND, Lx, VOUT and inductor. The wiring of output voltage setting resistance (R1) and the wiring of inductor must be separated from load wiring.
- The ceramic capacitors with low ESR (Equivalent Series Resistance) must be used for the ICs. The recommended value for the C_{IN} capacitor between VIN and GND is equal or more than 10 µF.
- The selections of inductor (L) and output capacitor (C_{OUT}) can be different according to the ICs' oscillation frequencies, output voltages and input voltages. Refer to "Recommended Value for Each Output Voltage" on the next page and select the most suitable values at the conditions of use.
- The internal phase compensation is built in the ICs; therefore, if the values selected are largely deviated from the recommended values, the operation may result in unstable.
- The over current protection circuit could be influenced by self-heating of the ICs and heat dissipation of the PCB environment.
- In order to prevent self-turning on, FET with smaller gate resistance and with smaller C_{GD}/ C_{GS} (capacities between gate drains and the capacities between gate sources) should be selected.
- The output voltage (V_{OUT}) can be calculated as $V_{OUT} = V_{FB} \times (R1 + R2) / R2$. The various voltage settings are possible by changing the values of R1 and R2. However, R2 value must be equal or less than 16 kΩ.
- R_{SPD} prevents the deterioration in the regulation characteristics, which is caused by spike noise occurred in VOUT. Spike noise is largely depending on the PCB layout. If the PCB board layout is optimized, there is no need of R_{SPD}; however, if the spike noise is a concern, R_{SPD} with 15 Ω or so should be used.
- The ICs are not supporting Nonsynchronous rectification using a diode as a rectifier.

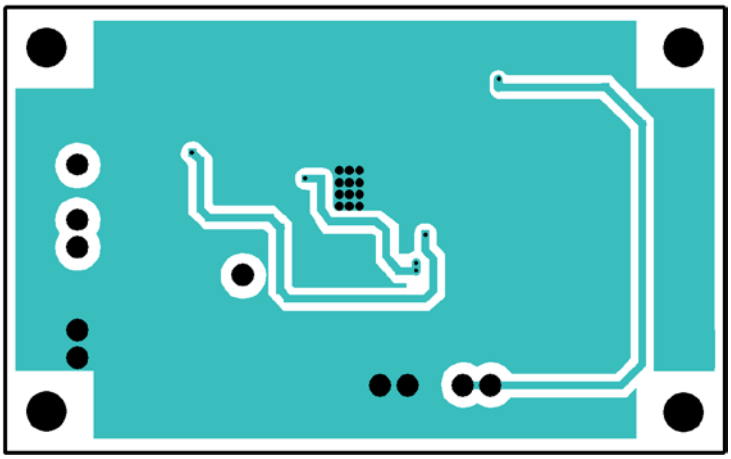
TECHNICAL NOTES ON PCB LAYOUT PATTERN

1. Make the power line (VIN and GND) broad to avoid the generation of the parasitic inductance. Place the bypass capacitor (C_{IN}) between VIN and GND as close as possible to each other.
2. Make the wire between Lx pin and the inductor as short as possible to avoid the generation of the parasitic inductance. (This Evaluation Board is designed for the testing. Therefore, the inductor is large, a diode is connectable, and the large space is secured for Lx part.)
3. The ripple current passes through the output capacitor; therefore, if the C_{OUT}'s GND is placed in the outside of the C_{IN}'s GND side and the IC's GND, the IC can be easily affected by the noise.
4. Mount R_{UP}, R_{BOT}, C_{SPD} and R_{SPD} on the place where the FB pin is close and the inductor and the BST pin are away.
5. Start the feedback from where the output capacitor (C_{OUT}) is close.

TOP VIEW



BOTTOM VIEW



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