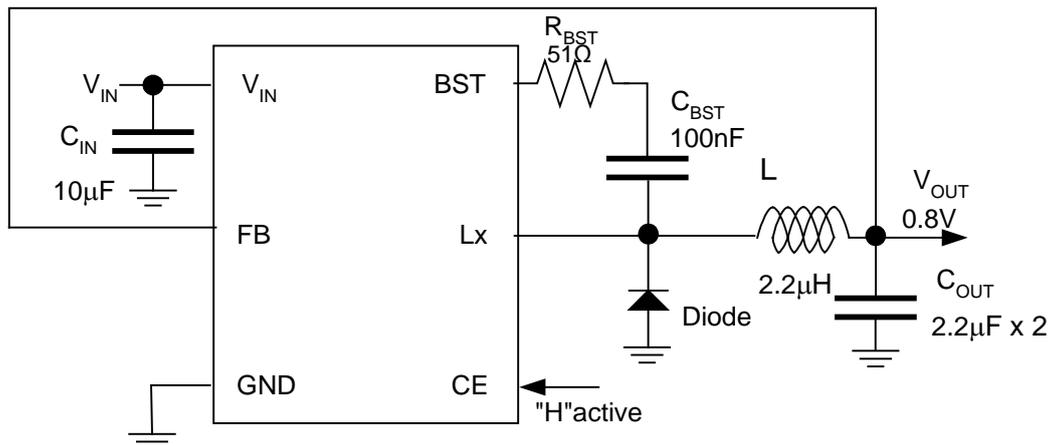


Design Guide

NO.ED-190-160630

Typical Application Circuit and Technical Notes for PCB

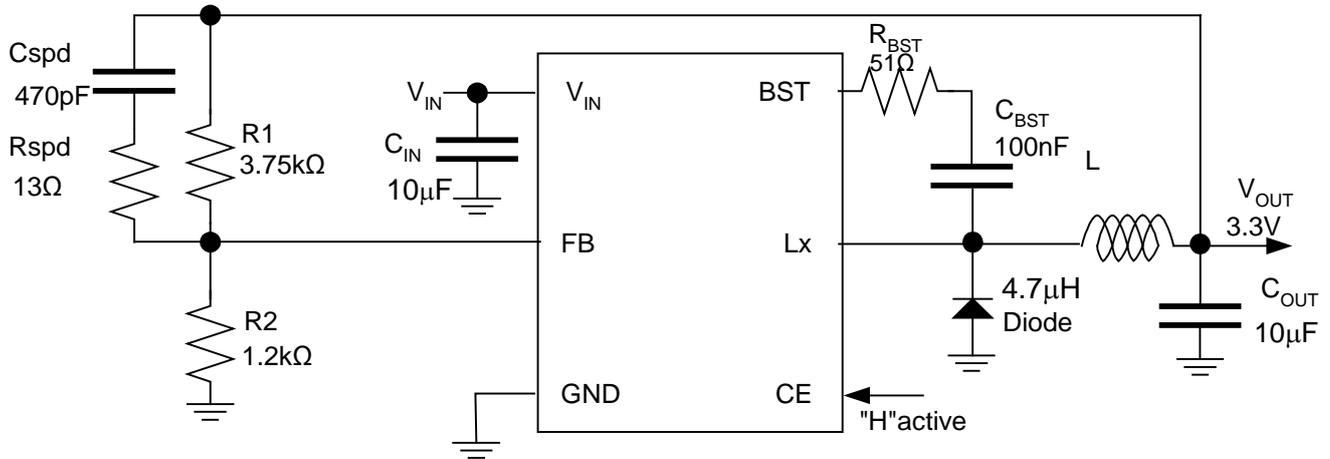
$V_{OUT}=0.8V$



Recommended External Components

C_{IN}	10µF KTS500B106M55N0T00 (Nippon Chemi-Con)
C_{OUT}	22µF x 2 GRM31CR71A226M (Murata)
C_{BST}	0.1µF GRM21BB11H104KA01L (Murata)
L	2.2µH VLCF4020T-2R2N1R7 (TDK)
Diode	CMS06 (Toshiba)

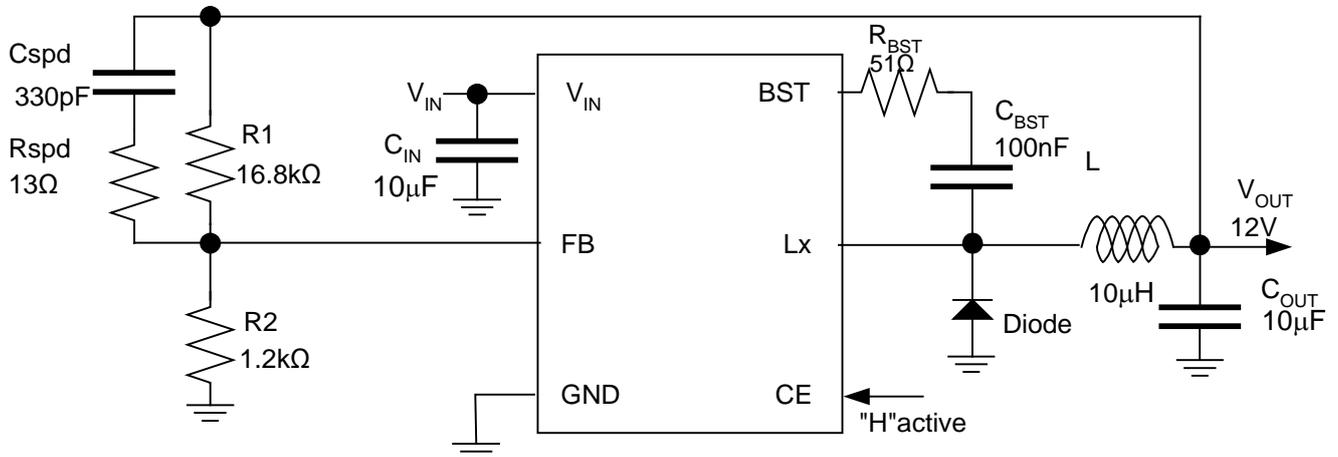
$V_{OUT}=3.3V$



Recommended External Components

C_{IN}	10 μ F KTS500B106M55N0T00 (Nippon Chemi-Con)
C_{OUT}	10 μ F GRM31CR71E106K (Murata)
C_{BST}	0.1 μ F GRM21BB11H104KA01 (Murata)
L	4.7 μ H SLF7045T-4R7M2R0-PF (TDK)
Diode	CMS11 (Toshiba)

$V_{OUT}=12V$



Recommended External Components

C_{IN}	10 μ F KTS500B106M55N0T00 (Nippon Chemi-Con)
C_{OUT}	10 μ F KTS500B106M55N0T00 (Nippon Chemi-Con)
C_{BST}	0.1 μ F GRM21BB11H104KA01L (Murata)
L	10 μ H SLF6045T-100M1R6-3PF (TDK)
Diode	CMS11 (Toshiba)

Technical Notes on External Parts

External components must be connected as close as possible to the ICs and make wiring as short as possible. Especially, the capacitor connected in between V_{IN} and GND pins must be wiring the shortest. The operating may be unstable due to the change of the electric potential of internal ICs by the switching current when the impedance of the power supply line and GND line is high. Make the power supply and GND lines sufficient. It is also necessary to give careful consideration to design the wiring of the power supply, GND, Lx, V_{OUT} and the inductor because of the large current by the function of switching is flowing into them. Besides, the wiring between the resistance (R1), which set the output voltage, and the wiring of the inductor must separate from the load wiring.

Capacitors with low ESR (Equivalent Series Resistance) such as ceramic capacitors are recommended for the ICs. The recommendation of C_{IN} capacitor between V_{IN} and GND is equal or more than $10\mu\text{F}$, and the recommendation of C_{OUT} capacitor is equal or more than $10\mu\text{F}$ in the case of $V_{OUT} \geq 1.8\text{V}$, while equal or more than $20\mu\text{F}$ in the case of $1.8\text{V} > V_{OUT}$. The dependence on DC bias and the temperature characteristics of the ceramic capacitors must be considered.

Select the inductor value in the range between $4.7\mu\text{H}$ and $10\mu\text{H}$ in the case of $V_{OUT} \geq 5\text{V}$, $4.7\mu\text{H}$ in the case of $5\text{V} > V_{OUT} \geq 1.8\text{V}$, and $2.2\mu\text{H}$ in the case of $1.8\text{V} > V_{OUT}$. The internal phase compensation of this IC is designed with the above-mentioned inductor value and C_{OUT} ceramic capacitor value. If the inductor value is small, there may be a cause of undesirable operation of over-current protection circuit by increasing of the peak switching current. Because if the inductor value is too small, as the load current increases, the switching peak current also easy to increase, as a result, the peak current may reach the current limit.

Note that the over-current protection circuit has temperature characteristics. Therefore, the circuit is easy to be affected by the heat generation of the ICs itself and heat radiation environment.

Select a Schottky diode with small C_j . If the C_j value is too large, during the on time of the switching, large switching current may flow and unstable operation may result.

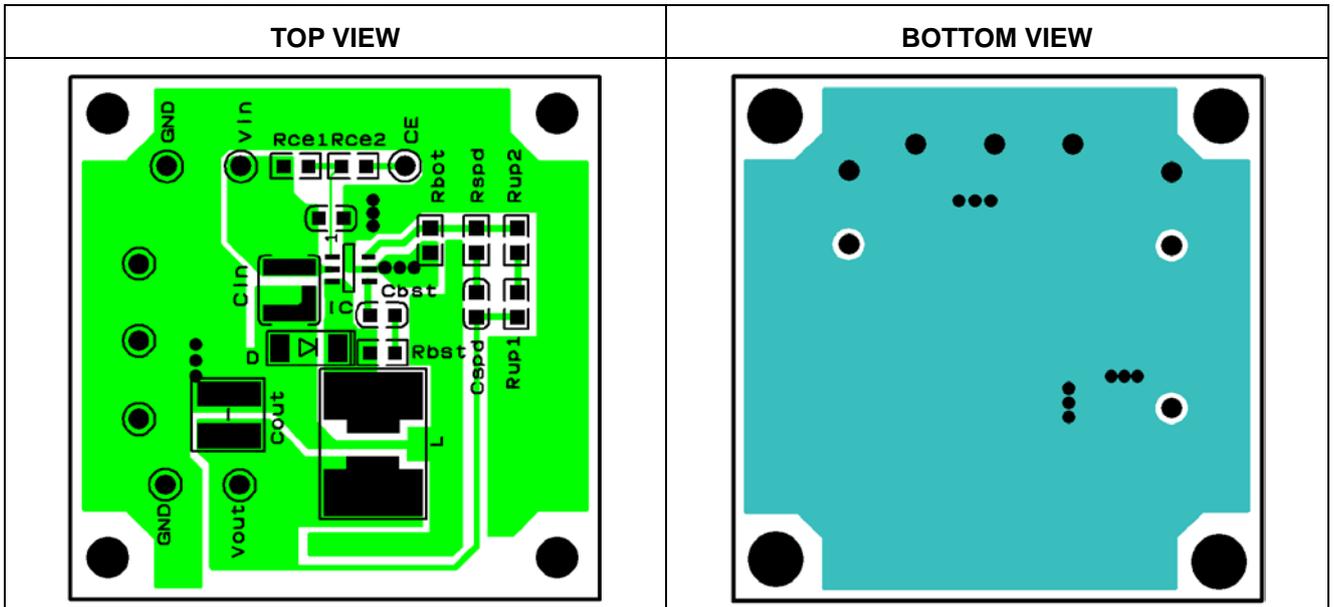
The performance of the power circuit with this IC largely depends on external components and circuit.

Select appropriate external components, especially, be sure not to exceed each rating (voltage, current, and power) of the IC and each component and the layout pattern must be considered to secure the power dissipation.

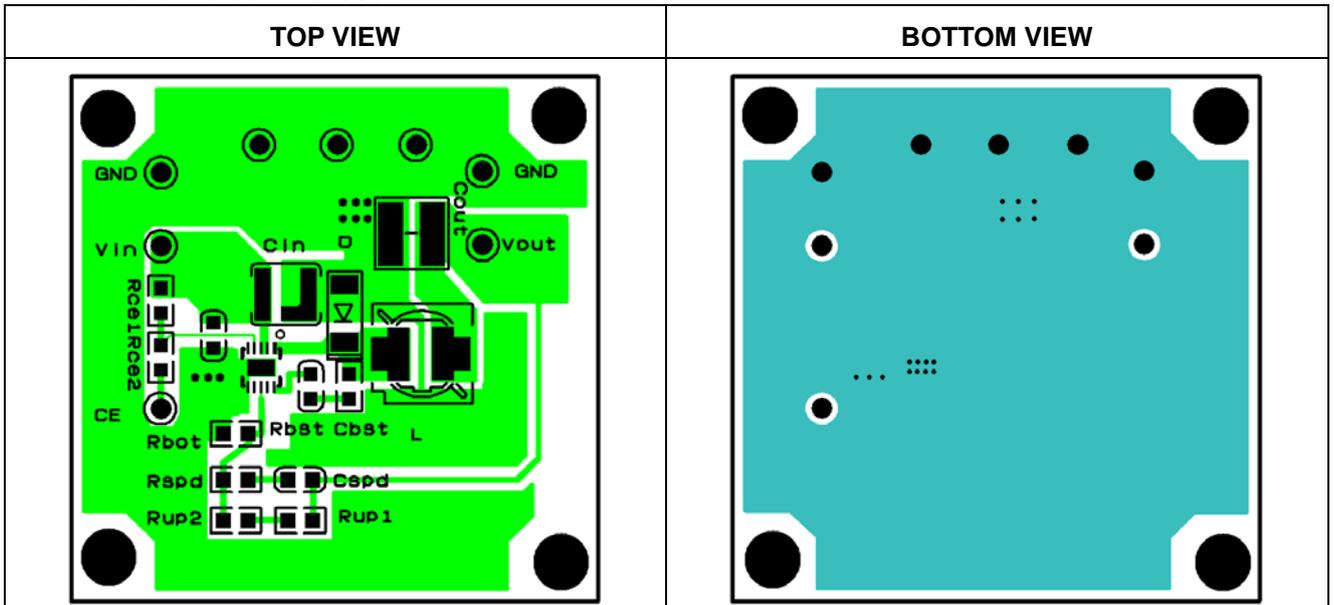
The Note of Layout Pattern

1. The wire of Power line (V_{IN} , GND) should be broad to minimize the parasitic inductance. The Bypass capacitor must be connected as close as possible in between V_{IN} – GND
2. The wire between Lx pin and the inductor as short as possible to minimize the parasitic inductance (This Evaluation Board is designed for the product evaluation board. Therefore large inductors or diodes can be set and the large space of Lx area has been secured.)
3. The ripple current flows through the output capacitor. If the GND side of the output capacitor is connected very close to GND pin of the IC, the noise might have a bad impact on the IC. Therefore, the GND side of the output capacitor is better to connect to the outside of the GND of the C_{IN} , or connect to the GND plain layer.
4. R1, R2, Cspd and Rspd should be mounted on the position as close as possible to the FB pin, and away from the inductor and BST pin.
5. The feed-back must be made as close as possible from the Output capacitor (C_{OUT})

Evaluation board of R1240N001x



Evaluation board of R1240K003x





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RICOH RICOH ELECTRONIC DEVICES CO., LTD.

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Sales & Support Offices

RICOH ELECTRONIC DEVICES CO., LTD.

Higashi-Shinagawa Office (International Sales)
3-32-3, Higashi-Shinagawa, Shinagawa-ku, Tokyo 140-8655, Japan
Phone: +81-3-5479-2857 Fax: +81-3-5479-0502

RICOH EUROPE (NETHERLANDS) B.V.

Semiconductor Support Centre
Prof. W.H. Keesomlaan 1, 1183 DJ Amstelveen, The Netherlands
Phone: +31-20-5474-309

RICOH INTERNATIONAL B.V. - German Branch

Semiconductor Sales and Support Centre
Oberrather Strasse 6, 40472 Düsseldorf, Germany
Phone: +49-211-6546-0

RICOH ELECTRONIC DEVICES KOREA CO., LTD.

3F, Haesung Bldg, 504, Teheran-ro, Gangnam-gu, Seoul, 135-725, Korea
Phone: +82-2-2135-5700 Fax: +82-2-2051-5713

RICOH ELECTRONIC DEVICES SHANGHAI CO., LTD.

Room 403, No.2 Building, No.690 Bibo Road, Pu Dong New District, Shanghai 201203, People's Republic of China
Phone: +86-21-5027-3200 Fax: +86-21-5027-3299

RICOH ELECTRONIC DEVICES CO., LTD.

Taipei office
Room 109, 10F-1, No.51, Hengyang Rd., Taipei City, Taiwan (R.O.C.)
Phone: +886-2-2313-1621/1622 Fax: +886-2-2313-1623