Design Guide

NO.ED-278-151014

Typical Application

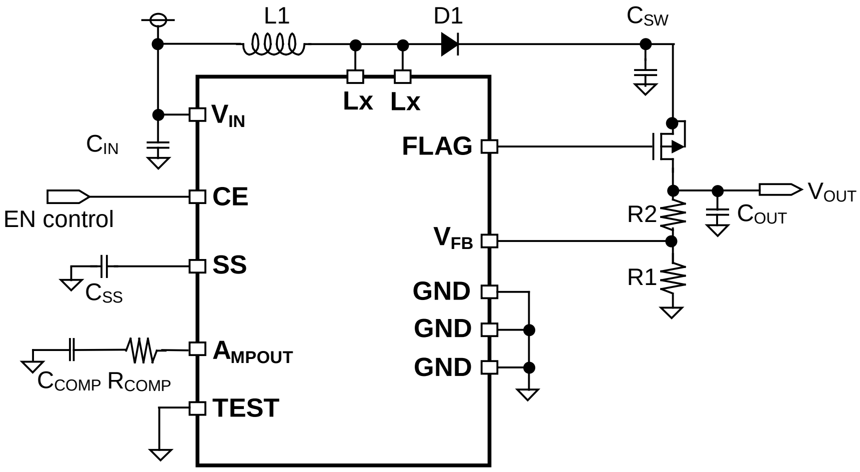

Figure 1. Circuitry with a Complete Shutdown Function

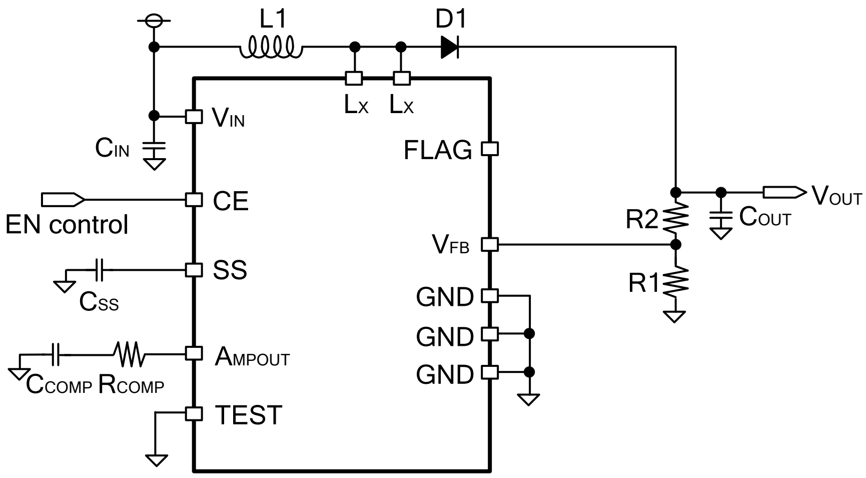

Figure 2. Circuitry without a Complete Shutdown Function

Recommended Components

Table 1.

	V_{IN}	Cap.	Spec.	Part Name	Manufacturer
C_{IN}	all	10µF	6.3V	C2012JB0J106M	TDK

	V_{OUT}	Cap.	Spec.	Part Name	Manufacturer
C_{OUT}	≤ 5V	10µF	6.3V	C2012JB0J106M	TDK
	≤10V	10µF	16V	C2012X5R1C106K	TDK
	all	10µF	25V	C3216X5R1E106K	TDK
	all	10µF	25V	TMK325BJ106MN	Taiyo Yuden

	V_{OUT}	Spec.	Part Name	Manufacturer
D1	all	40V 3A	CMS16	TOSHIBA
	all	40V 3A	RB056L-40	ROHM

	V_{OUT}	Ind.	Spec.	Part Name	Manufacturer
L1(1)	3.0V≦V_{OUT}≦4.5V	2.2µH	2.2A	SPM3012T-2R2N	TDK
			2.7A	SPM4012T-2R2N	TDK
			3.5A	NR5040T2R2N	Taiyo Yuden
	4.5V＜V_{OUT}≦12V	4.7µH	1.7A	SPM4012T-4R7N	TDK
			3.1A	NR5040T4R7N	Taiyo Yuden
	12V＜V_{OUT}≦15V	6.8µH	1.4A	VLF5014ST-6R8N	TDK
			2.8A	RLF7030T-6R8N	TDK
			3.7A	NR8040T6R8N	Taiyo Yuden

	V_{OUT}	Spec. (I_{DS}, V_{DS}, V_{GS})	Part Name	Manufacturer
Pch MOSFET(2)	all	4.5A, -30V, ±20V	UPA1914	Renesas

	Cap.	Spec	Part Name	Manufacturer
C_{SW}(2)	1µF	25V	C1608JB1E105K	TDK

(1) It is recommended that the inductor (L1) with an inductance of more than the L_X current limit be used. In case of using another device for current limiting, L1 less than the L_X current limit can be used.
(2) When using a complete shutdown switch control pin (FLAG pin) for complete shutdown, place a Pch MOSFET and a C_{SW}. Refer to the typical application.

Technical Notes

- The R1213K001x includes a timer latch protection circuit. If the output voltage drop due to the overcurrent continues for more than the protection delay time, the latch time protection circuit latches the built-in driver off and stops the DC/DC converter operation. When the timer latch protection circuit is triggered, the complete shutdown switch control pin outputs a "H" signal, and turns the Pch MOSFET off if it is connected, in order to shutdown the current path from the power supply to the output.
- The protection delay time is set to Typ. 32ms. If the output voltage is recovered during the protection delay time, the built-in timer will be reset.
- To release the protection delay time, input a "L" signal to the CE pin or decrease the supply voltage lower than the UVLO detector threshold.
- The TEST pin must be connected to GND or be left open.
- The complete shutdown switch control pin (the FLAG pin) can only be used for the purpose of shutdown. When using the FLAG pin, it must be connected to the gate of an external Pch MOSFET; do not use this pin for other purposes.
- To prevent the inrush current, place an appropriate capacitor to the SS pin. The SS pin can only be used for the purpose of soft-start; do not use this pin for other purposes.

★ The exposed pad on the bottom of the package enhances the thermal performance and is electrically connected to GND inside the package. It is recommended that the exposed pad be connected to the ground plane on the board with thermal vias if possible.

External Components

- Ensure that the V_{IN} and GND lines are sufficiently robust considering the large switching current. If the impedances of the V_{IN} and GND lines are too high, the switching current may shift the internal voltage level and cause the device operation unstable. When the internal L_X switch turns off, spike noise may be generated by the inductor. Therefore, it is recommended that the output capacitor (C_{OUT}) voltage and diode be more than 1.5 times of preset output voltage.

- Choose an appropriate diode with low Vf (such as Schottky barrier diode), low IR, and fast switching speed.

- Choose an appropriate inductor with low DC resistance, sufficient permissible current, and which is hard to reach magnetic saturation type.

- In this IC, the complete shutdown switch control pin is built in. The IC controls an external P-channel MOSFET to make complete shutdown when the IC must be standby, detecting UVLO, thermal shutdown, and timer latch protection. Therefore the current path between power supply and the output can be completely cut off. For using this function, a P-channel MOSFET must be used, FLAG pin output turns off the MOSFET and the over voltage which is generated on the source pin of the MOSFET by the inductor current must be cared. Therefore, put a 1µF capacitor (C_{SW}) between the source of the MOSFET and GND.
  During the soft-start time at ramp-up, the signal of the FLAG pin is synchronized with the internal switching, and turns on and off the P-channel MOSFET and prevent the inrush current. Therefore choose an appropriate external P-channel MOSFET with fast switching speed(tr is equal or less than 100ns), and small gate capacitance (3nF or less).

- The spike noise of the L_X must not be beyond the absolute maximum rating. If the spike noise is too large, set a snub circuit (Ex. CR in serial) in parallel to the diode D1 to reduce the noise. The appropriate value of CR depends on the actual PCB, and may have some effect on the efficiency, therefore evaluate and determine the final value with the actual PCB. (The basic value is 10Ω and 300pF, therefore, start the evaluation from these values and adjust the appropriate values.)

★ The performance with using this IC largely depends on the peripheral circuits or external components. Especially, external components, PCB layout and for this IC, fully consideration of not being beyond the absolute maximum ratings such as voltage, current, and power is necessary to design.

Board Layout Example

Current Path on the PCB

In Fig.1 and Fig.2, the current paths on the boost DC/DC converter are shown. The current paths when the MOSFET turns on are shown in Fig. 1, and the current paths when the MOSFET turns off are shown in Fig. 2. The pointed parts with red arrows in Fig. 2 are where the current flows only when the MOSFET turns on, or off. The parasitic impedance, inductance, or parasitic capacitance of these parts have some impact on the stability of DC/DC converter, and may cause a noise generation. Therefore the parasitic impedance, capacitance, inductance must be as small as possible. Furthermore, the current paths shown in Fig.1 and Fig.2 must be as short as possible and as wide as possible.

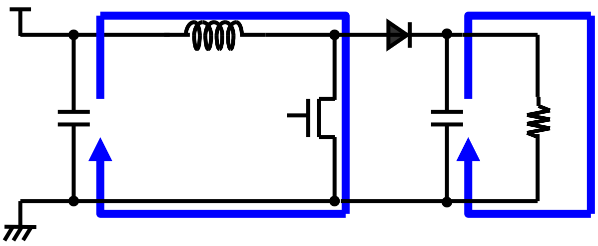

Figure 3. MOSFET-ON (Boost)

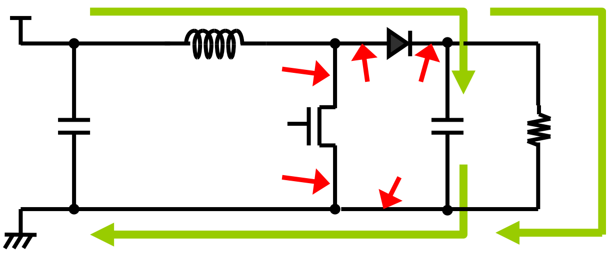

Figure 4. MOSFET-OFF (Boost)

R1213K001A/B (PKG: DFN(PLP)2730-12pin) Circuitry with a Complete Shutdown Function

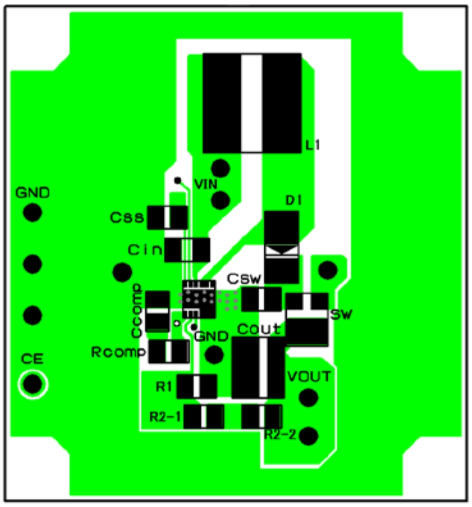

Figure 5. Typical Board Layout – Top Side

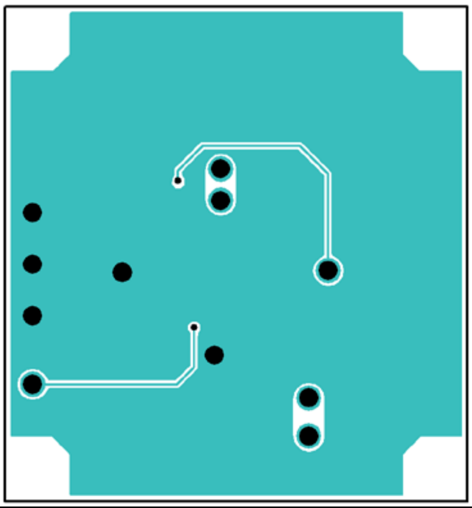

Figure 6. Typical Board Layout – Bottom Side

Note: R2 patterns are the layout for 2 serial resistance chips, R2-1 and R2-2 to set preferred value easier.

R1213K001A/B (PKG: DFN(PLP)2730-12pin) Circuitry without a Complete Shutdown Function

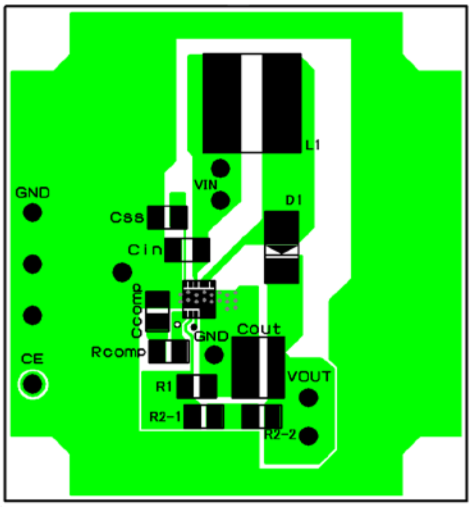

Figure 7. Typical Board Layout – Top Side

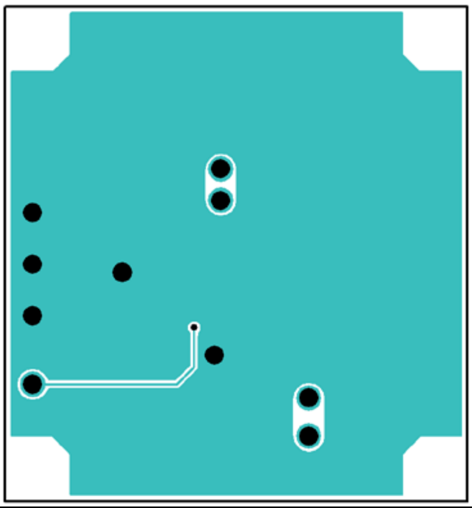

Figure 8. Typical Board Layout – Bottom Side

Note: R2 patterns are the layout for 2 serial resistance chips, R2-1 and R2-2 to set preferred value easier.

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