Design Guide

NO.ED-192-130919

■ TYPICAL APPLICATION

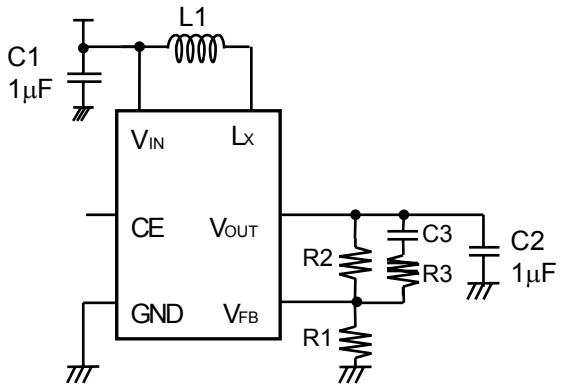


Fig.1

●Selection of Inductors

The peak current of the inductor at normal mode can be estimated as the next formula when the efficiency is 80%.

I_{LXmax}=1.25 x I_{LED} x V_{OUT} / V_{IN} + 0.5 x V_{IN} x (V_{OUT} - V_{IN}) / (L x V_{OUT} x fosc)

In the case of start-up or dimming control by CE pin, inductor transient current flows, and the peak current of it must be equal or less than the current limit of the IC. The peak current should not beyond the rated current of the inductor.
The recommended inductance value is 10-22μH.

Table 1 Peak current value in each condition

Condition				
V_{IN}(V)	V_{OUT}(V)	I_{OUT}(mA)	L(μH)	I_{LXmax}(mA)
3	14	20	10	215
3	14	20	22	160
3	21	20	10	280
3	21	20	22	225

Table 2 Recommended inductors

L (μH)	Part No.	Rated current(mA)	Size (mm)
10	LQH32CN100K53	450	3.2x2.5x1.55
10	LQH2MC100K02	225	2.0x1.6x0.9
10	VLF3010A-100	490	2.8x2.6x0.9
10	VLS252010-100	520	2.5x2.0x1.0
22	LQH32CN220K53	250	3.2x2.5x1.55
22	LQH2MC220K02	185	2.0x1.6x0.9
22	VLF3010A-220	330	2.8x2.6x0.9

●Selection of Capacitors

Set 1μF or more value bypass capacitor C1 between V_{IN} pin and GND pin as close as possible.
Set 1μF – 4.7μF or more capacitor C2 between V_{OUT} and GND pin.

Table 3 Recommended components

	Rated voltage(V)	Part No.
C1	6.3	CM105B105K06
C2	25	GRM21BR11E105K
C3	25	220pF
R1		For V_{OUT} Setting
R2		For V_{OUT} Setting
R3		2kΩ

■ TYPICAL BOARD LAYOUT

●Current path on PCB

The current paths in an application circuit are shown in Fig.2 and 3.
A current flows through the paths shown in Fig.2 at the time of MOSFET-ON, and shown in Fig.3 at the time of MOSFET-OFF. In the paths pointed with red arrows in Fig.3, current flows just in MOSFET-ON period or just in MOSFET-OFF period. Parasitic impedance / inductance and the capacitance of these paths influence stability of the system and cause noise outbreak. So please minimize this side effect. In addition, please shorten the wiring of other current paths shown in Fig.2 and 3 except for the paths of LED load.

●LAYOUT Guide for PCB

・ Please shorten the wiring of the input capacitor(C1) between V_{IN} pin and GND pin of IC. The GND pin should be connected to the strong GND plane.

・ The area of L_X land pattern should be smaller.

・ Please put output capacitor(C2) close to the V_{OUT} pin.

・ Please make the GND side of output capacitor(C2) close to the GND pin of IC.

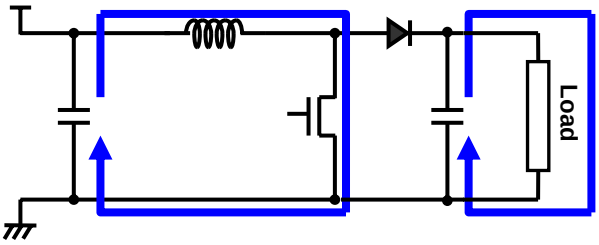


Fig.2 MOSFET-ON

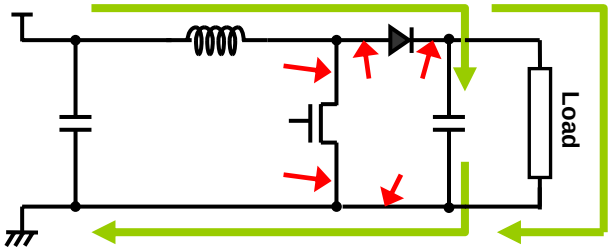
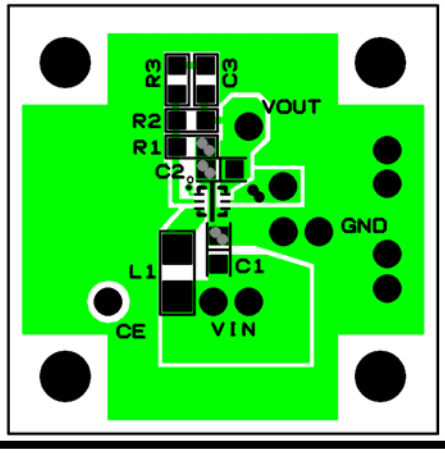
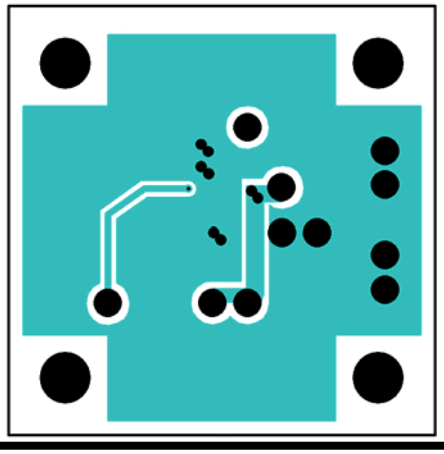


Fig.3 MOSFET-OFF

Board Layout

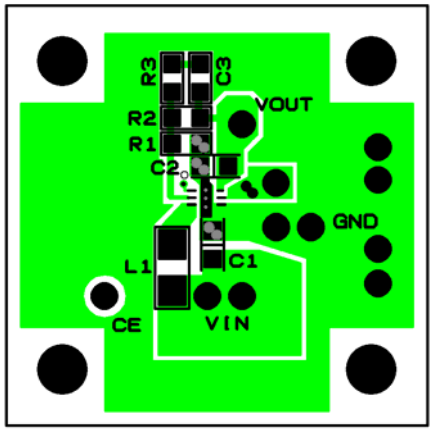
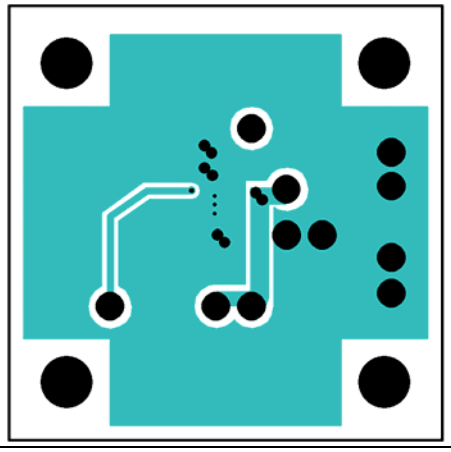
・ PKG:DFN1616-6pin

R1200L typical board layout

Topside	Backside
	

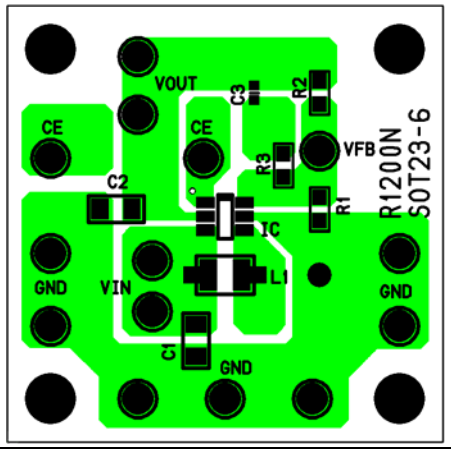
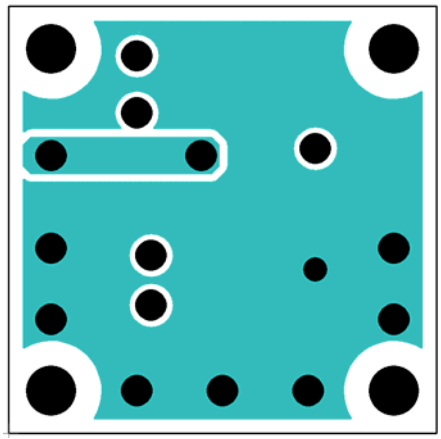
・PKG:DFN(PLP)1820-6pin

R1200K typical board layout

Topside	Backside
	

・PKG:SOT-23-6pin

R1200N typical board layout

Topside	Backside
	

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