POWER MANAGEMENT IC

RD5T7319

Simplified Specifications

Rev. 1.0

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RICOH COMPANY, LTD.
Electronic Devices Company

This specification is subject to change without notice.

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1. Outline

RD5T7319 is the power management IC. It integrates four high-efficiency DCDC (step-down x 2ch, buck-boost x 2ch) converters, four low-jitter ClockGenerator outputs, power control logic, voltage detections, thermal shutdown, UVLO and etc.

2. Feature

- High-efficiency DC/DC Converters x4ch
  - ✓ DCDC1: 1.5 /1.8V @ 2.0A (step-down)
  - ✓ DCDC2: 3.3V @ 0.6A (buck-boost)
  - ✓ DCDC3: 1.1 /1.15V @ 2.0A (step-down)
  - ✓ DCDC4: 1.2 /1.5 /1.8 /3.3 /5V @ 0.6A (buck-boost)

- Voltage Detectors
  - ✓ UVLO: monitors the VDD1 pin voltage (for RD5T7319 operation)
  - ✓ VINDET: monitors the VDD1 pin voltage
  - ✓ RTCDET: monitors the VSB pin voltage
  - ✓ DETIO: monitors the VDDIO2 pin voltage

- Serial Interface (I2C-BUS)
  - ✓ Fast-mode (100 kHz/400 kHz) support

- Real-Time Clock (RTC)
  - ✓ Alarm function
  - ✓ Coin charge regulator: 3.3V @10mA (For coin battery or capacitor)
  - ✓ One 32.768kHz CMOS output pin

- Interrupt Controller (INTC)
  - ✓ Alarm interrupt and Periodic interrupt from RTC
  - ✓ And other interrupt

- Reset Control
  - ✓ The reset is generated from RESETB and L0DET pin
  - ✓ External reset signal detection

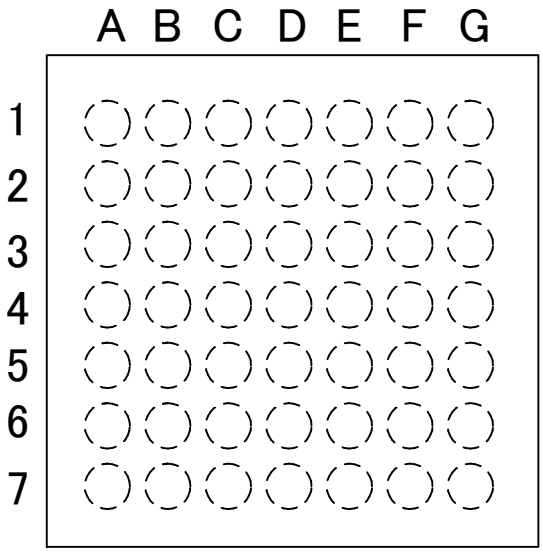
- Clock Generator
  - ✓ Two integrated phase-locked loops
  - ✓ Four configurable and low jitter outputs

- Package
  - ✓ 49pin WLCSP-package (3.5mm x 3.5mm pin 0.5mm pitch)

- Process
  - ✓ CMOS Process

3. Pin Configuration

WLCSP, Size 3.50mm x 3.50mm, 49pins, 0.5mm pitch



	A	B	C	D	E	F	G
1	OSCOUT	OSCIN	VINT	DD2VOUT	DD2SWIN	**GNDDD2**	DD2SWOUT
2	XOUT	**VDDIO2**	SCL	DD2VFB	**GNDIOCK**	**VDDIO1**	**VINDD2**
3	XIN	**GNDCK**	CLKO1	SDA	L0DET	DD1VFB	**GNDDD1**
4	**VSB**	VREFO	CLKO3	CLKO2	C32KOUT	LOWPWR	DD1LX
5	CKVIO	**VDD1**	**GND2**	CLKO4	EXTRSTB	RESETB	**VINDD1**
6	**VINDD4**	SEL1	SEL2	DD4VFB	**GND1**	INTOUTB	DD3VFB
7	DD4SWOUT	**GNDDD4**	DD4SWIN	DD4VOUT	**VINDD3**	DD3LX	**GNDDD3**

Table 3-1 Pin Description (Bottom View)

4. Block Diagram

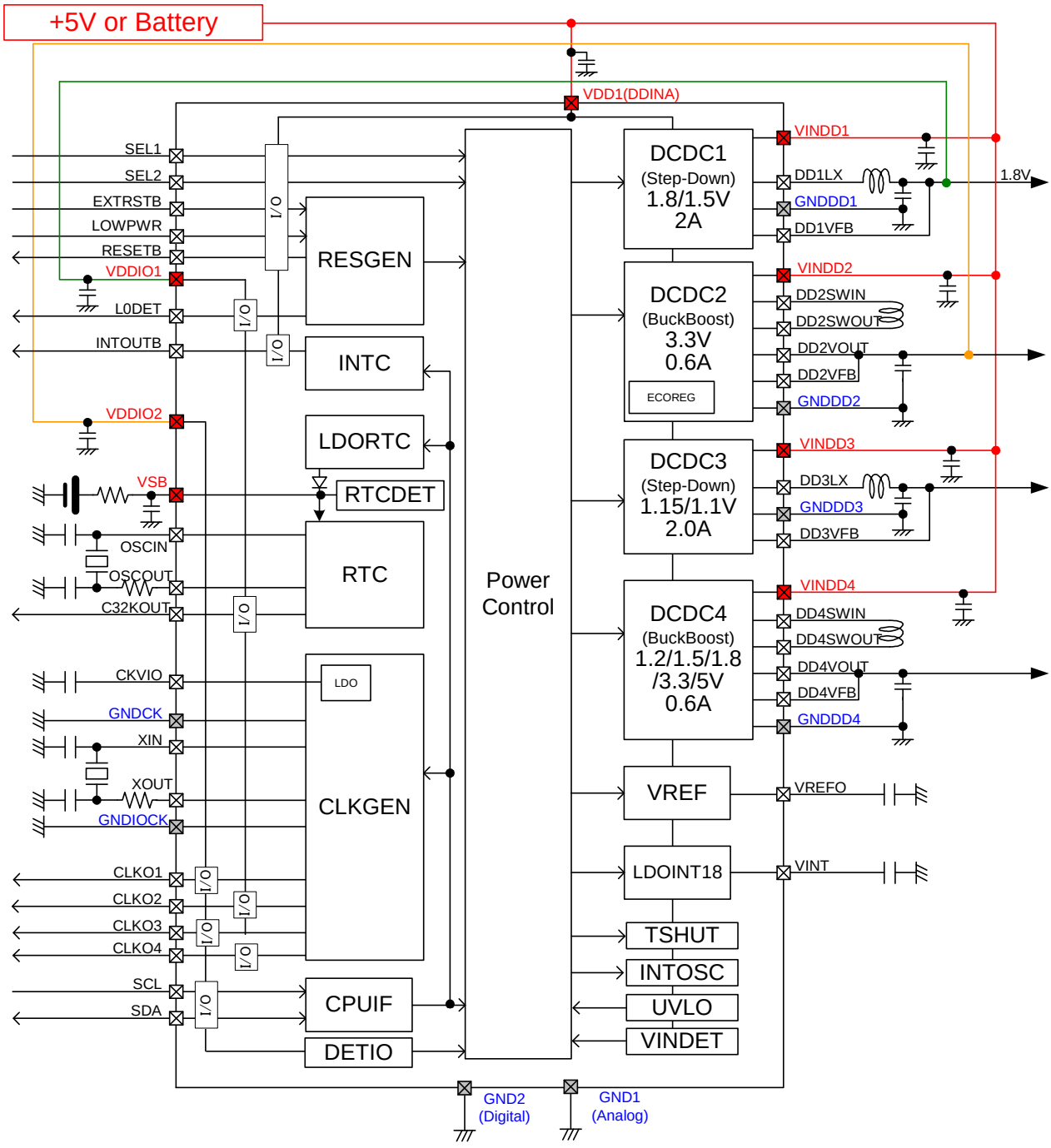


Fig. 4-1 Block Diagram

5. Pin Description

Total	Ball No.	Name	Block	Function	I/O	D/A	Type		PU/PD	I/F Voltage	Initial Value	Note
							input	output				
1	G5	VINDD1	DCDC1	Power supply for DCDC1 driver	-	P	-	-	-	-	-	
2	G3	GNDDD1	(1.8/1.5V)	GND for DCDC1 driver	-	G	-	-	-	-	-	
3	G4	DD1LX		DCDC1 switch output	O	A	-	-	-	-	-	
4	F3	DD1VFB		DCDC1 Output voltage feedback input	I	A	-	-	-	1.5/1.8V	-	
5	G2	VINDD2	DCDC2	Power supply for DCDC2 driver	I	P	-	-	-	-	-	
6	F1	GNDDD2	(3.3V)	GND for DCDC2 driver	-	G	-	-	-	-	-	
7	D1	DD2VOUT		DCDC2 output	O	A	-	-	-	3.3V	-	
8	D2	DD2VFB		DCDC2 Output voltage feedback input	I	A	-	-	-	-	-	
9	E1	DD2SWIN		DCDC2 SW input	I	A	-	-	-	-	-	
10	G1	DD2SWOUT		DCDC2 SW output	O	A	-	-	-	-	-	
11	E7	VINDD3	DCDC3	Power supply for DCDC3 driver	I	P	-	-	-	-	-	
12	G7	GNDDD3	(1.1/ 1.15V)	GND for DCDC3 driver	-	G	-	-	-	-	-	
13	F7	DD3LX		DCDC3 switch output	O	A	-	-	-	-	-	
14	G6	DD3VFB		DCDC3 Output voltage feedback input	I	A	-	-	-	1.1/1.15V	-	
15	A6	VINDD4	DCDC4	Power supply for DCDC4 driver	I	P					-	
16	B7	GNDDD4		GND for DCDC4 driver	-	G	-	-	-	-	-	
17	D7	DD4VOUT	(1.2/1.5/1.8	DCDC4 output	O	A	-	-	-	1.2/1.5/1.8/ 3.3/5V	-	
18	D6	DD4VFB	3.3//5V)	DCDC4 Output voltage feedback input	I	A	-	-	-	-	-	
19	C7	DD4SWIN		DCDC4 SW input	I	A	-	-	-	-	-	
20	A7	DD4SWOUT		DCDC4 SW output	O	A	-	-	-	-	-	
21	B5	VDD1	Power	Power supply	-	P	-	-	-	-	-	
22	F2	VDDIO1		Power supply for I/O pin 1	-	P	-	-	-	1.8/3.3V	-	
23	B2	VDDIO2		Power supply for I/O pin 2	-	P	-	-	-	3.3V	-	
24	E6	GND1		GND for Analog	-	G	-	-	-	-	-	
25	C5	GND2		GND for Digital	-	G	-	-	-	-	-	
26	C1	VINT		LDOINT18 output (for internal logic)	O	A	-	-	-	1.8V	-	
27	B4	VREFO		Bypass capacitor connecting pin	O	A	-	-	-	-	-	
28	F5	RESETB	RESET	Reset signal output pin	O	D	-	NchOD (2mA)	-	VDD1	Low	At the Backup State of PMU, leakage current may occur into the internal circuit if a pin is externally pulled up.
29	E3	L0DET		Buck DCDC3 power-on signal output pin	O	D	-	CMOS (4mA)	-	VDDIO1	Hi-z	Initial Value is "Low",when VDDIO1 is operating conditions.
30	E5	EXTRSTB		External reset signal detection pin	I	D	Nch	-	-	VDD1	-	External Pull-up resistance. Pushed Switch or CMOS input.
31	F4	LOWPWR		External reset signal detection pin	I	D	Nch	-	-	VDD1	-	
32	F6	INTOUTB	INTC	Interrupt output pin	O	D	-	NchOD (2mA)	-	VDD1	Hi-z	At the Backup State of PMU, leakage current may occur into the internal circuit if a pin is externally pulled up.
33	B6	SEL1	PWRCTL	Select pin 1	I	D	CMOS	-	-	GND/VDD1	-	
34	C6	SEL2		Select pin 2	I	D	CMOS	-	-	GND/VDD1	-	
35	B1	OSCIN	RTC	32kHz oscillation clock input	I	A	-	-	-	-	-	
36	A1	OSCOUT		32kHz oscillation clock output	O	A	-	-	-	-	-	
37	A4	VSB		LDORTC output / Coin-Battery (for RTC)	I/O	A/P	-	-	-	-	-	
38	E4	C32KOUT		RTC Clock output pin	O	D	-	CMOS (4mA)	-	VDDIO1	Hi-z	Initial Value is "Low",when VDDIO1 is operating conditions.
39	C2	SCL	CPUIF	serial clock bus	I	D	CMOS Schmitt	-	-	VDDIO2	-	5.5V tolerant input
40	D3	SDA		serial data bus	I/O	D	CMOS Schmitt	NchOD (3mA)	-	VDDIO2	Input	5.5V tolerant input
41	A5	CKVIO	CLKGEN	Bypass capacitor connecting pin (for internal PLL)	O	A	-	-	-	-	-	
42	B3	GNDCK		Analog GND for CLKGEN	-	G	-	-	-	-	-	
43	E2	GNDIOCK		Digital(I/O) GND	-	G	-	-	-	-	-	
44	A3	XIN		Oscillation clock input	I	A	-	-	-	VDDIO2	-	
45	A2	XOUT		Oscillation clock output	O	A	-	-	-	VDDIO2	-	
46	C3	CLKO1		Clock output1	O	D	-	CMOS (4mA)	-	VDDIO2	Hi-z	Initial Value is "Low",when VDDIO2 is operating conditions.
47	D4	CLKO2		Clock output2	O	D	-	CMOS (4mA)	-	VDDIO1	Hi-z	Initial Value is "Low",when VDDIO1 is operating conditions.
48	C4	CLKO3		Clock output3	O	D	-	CMOS (4mA)	-	VDDIO2	Hi-z	Initial Value is "Low",when VDDIO2 is operating conditions.
49	D5	CLKO4		Clock output4	O	D	-	CMOS (4mA)	-	VDDIO1	Hi-z	Initial Value is "Low",when VDDIO1 is operating conditions.

Table 5-1 Pin Description

Pin Type ("I/O" line)
I : Input Pin
O : Output Pin
I/O : Input Output Pin

Pin Type ("D/A" line)
D: Digital Pin
A: Analog Pin
P: Power Supply input Pin
G: GND

6. Regulator

6.1 DCDC Converter

DCDC1 and DCDC3, which are Synchronous Rectified Step-down DC/DC Converters, have a function to switch PFM/PWM automatically.
DCDC2 and DCDC4 are Fully-Synchonized Rectified Buck-Boost DC/DC Converters.

Following is explanation for the Auto mode and the fixed PWM.

Mode	Description
Auto	PFM/PWM modes are automatically switched depending on load current. When heavy load, PWM with the fixed frequency of 2.25MHz is selected. When light load, PFM is selected.
PWMFIX	Regardless of heavy/light load currents, PWM with the fixed frequency of 2.25MHz is selected. As for the Output ripple voltage and the Output transition response at the light load current, this mode has more advantages than the Auto mode. On the other hand, owing to the internal current consumption, the efficiency at the light load current becomes at the disadvantage compared to the Auto mode.

6.1.1 Step-down DCDC Converter (DCDC1)

DCDC1 (DCDC converter for Auto-swicth of PFM/PWM)

Auto Mode

Electrical Characteristics:

L=2.2μH, C_{IN} = 22μF, C_{OUT} = 22μF(Capacitor tolerance±20%/Temperature characteristic±10%), Ta=-30~85℃

Symbol	Parameter	Condition	Min	Typ	Max	Units
Vin	Input voltage range		2.9	5	5.5	V
Vout	Output voltage accuracy	2.9V≦Vin≦5.5V, 10μA≦Iout≦2000mA	-2% -2%	1.5 1.8	+2% +2%	V
Fosc	Switching frequency			2.25		MHz
ILx	Maximum output current	2.9V≦Vin≦5.5V	2000			mA
ILxlim	Limit current	2.9V≦Vin≦5.5V		2500		mA
Vpeak	Output transition response	Vin=5V, Vout=1.8V 10mA→400mA@ΔT=1μs			100	mV
Tr	Rising time	Vout=1.8V, Iout=0mA			500	μs
Tf	Falling time	Iout=0mA			500	μs
Iss	Consumption current	Vin=5V, Iout=0mA		50		μA
VripO	Output ripple voltage	Vin=5V,Vout=1.8V, Iout=10mA		25		mV
		Vin=5V, Vout=1.8V, Iout=1A		10		mV
η1	Efficiency peak	Vin=5V, Vout=1.8V, Io＝0~Iomax		88		%

PWMFIX Mode

Symbol	Parameter	Condition	Min	Typ	Max	Units
Iss	Consumption current	Vin=5V, Iout=0mA		12		mA
VripO	Output ripple voltage	Vin=5V, Vout=1.8V, Iout=10mA		10		mV
		Vin=5V, Vout=1.8V, Iout=1A		10		mV
Vpeak	Output transition response	Vin=5V, Vout=1.8V 0mA→400mA@ΔT=1μs			100	mV
η1	Efficiency peak	Vin=5V, Vout=1.8V, Io=0~Iomax		88		%

6.1.2 Buck-Boost DCDC Converter (DCDC2)

DCDC2 (DCDC converter for Step-Up/Down)

Full-Synchronous Rectification

Electrical Characteristics:

L=1.5μH, C_{IN} = 10μF, C_{OUT} = 10μF (Capacitor tolerance±20% / Temperature characteristic±10%), Ta=-30~85℃

Symbol	Parameter	Condition	Min	Typ	Max	Units
Vin	Input voltage range		2.9	5	5.5	V
Vout	Output voltage accuracy	2.9V≦Vin≦5.5V, 10μA≦Iout≦600mA	-2%	3.3	+2%	V
	Range of output voltage		3.3		3.4	
Fosc	Switching frequency			3.0		MHz
ILx	Maximum output current	2.9V≦Vin≦5.5V	600			mA
ILxlim	Limit current	2.9V≦Vin≦5.5V		2000		mA
Vpeak	Output transition response	Vin=5V, Vout=3.3V 10mA→100mA@ΔT=1μs			200	mV
Tr	Rising time	Vout=3.3V, Iout=0mA			1	ms
Tf	Falling time	Iout=0mA			500	μs
Iss	Consumption current	Vin=5V, Iout=0mA		10		mA
VripO	Output ripple voltage	Vin=5V, Vout=3.3V, Iout=100mA		10		mV
η1	Efficiency peak	Vin=5V, Vout=3.3V, Iout=0~600mA		90		%

ECOREG

Symbol	Parameter	Condition	Min	Typ	Max	Units
Vin	Input voltage range		2.9	5	5.5	V
Vout	Output voltage range	Vout+0.2V≦Vin≦5.5V, 10μA≦Iout≦10mA	-3%	3.2	+3%	V
ILx	Maximum output current	Vout+0.2V≦Vin≦5.5V	10			mA
Iss	Consumption current	Vin=5V, IOUT=0mA		3	5	μA
Ilimit	Limit Current	Vout+0.2V≦Vin≦5.5V			200	mA

Note: ECOREG is available with “4.4≦Vin≦5.5V” condition, because of having a transient voltage distortion during the mode transition from ECOREG to DCDC.

6.1.3 Step-Down DCDC Converter (DCDC3)

DCDC3 (DCDC converter for Auto-swicth of PFM/PWM)

Auto Mode

Electrical Characteristics:

L=2.2μH, C_{IN} = 22μF, C_{OUT} = 22μF (Capacitor tolerance±20% / Temperature characteristic±10%), Ta=-30~85°C

Symbol	Parameter	Condition	Min	Typ	Max	Units
Vin	Input voltage range		2.9	5	5.5	V
Vout	Output voltage accuracy	2.9V≦Vin≦5.5V、10μA≦Iout≦2000mA	-2%	1.1	+2%	V
			-2%	1.15	+2%	
	Range of output voltage		0.75		1.375	
Fosc	Switching frequency			2.25		MHz
ILx	Maximum output current	2.9V≦Vin≦5.5V	2000			mA
ILxlim	Limit current	2.9V≦Vin≦5.5V		2500		mA
Vpeak	Output transition response	Vin=5V, Vout =1.15V 10mA→100mA@ΔT=1μs			25	mV
Tr	Rising time	Vout=1.15V, Iout=0mA			500	μs
Tf	Falling time	Iout=0mA			500	μs
Iss	Consumption current	Vin=5V, Iout=0mA		50		μA
VripO	Output ripple voltage	Vin=5V, Vout=1.15V, Iout=10mA		25		mV
		Vin=5V, Vout=1.15V, Iout=1A		10		mV
η1	Efficiency peak	Vin=5V, Vout=1.15V, Io=0~Iomax		84		%

PWMFIX Mode

Symbol	Parameter	Condition	Min	Typ	Max	Units
Iss	Consumption current	Vin=5V, Iout=0mA		12		mA
VripO	Output ripple voltage	Vin=5V, Vout=1.15V, Iout=10mA		10		mV
		Vin=5V, Vout=1.15V, Iout=1A		10		mV
Vpeak	Output transition response	Vin=5V, Vout=1.15V 0mA→100mA@ΔT=1μs			25	mV
η1	Efficiency peak	Vin=5V, Vout=1.15V, Io=0～Iomax		84		%

Note：Don't use PWMFIX mode during standby mode.（Vout < 1.0V）

6.1.4 Buck-Boost DCDC Converter (DCDC4)

DCDC4 (DCDC converter for Step-Up/Down)

Full-Synchronous Rectification

Electrical Characteristics:

L=1.5μH, C_{IN} = 10μF, C_{OUT} = 10μF (Capacitor tolerance±20% / Temperature characteristic±10%), Ta=-30~85℃

Symbol	Parameter	Condition	Min	Typ	Max	Units
Vin	Input voltage range		2.9	5	5.5	V
Vout	Output voltage accuracy	2.9V≦Vin≦5.5V、10μA≦Iout≦600mA	-2%	1.2	+2%	V
			-2%	1.5	+2%	
			-2%	1.8	+2%	
			-2%	3.3	+2%	
			-2%	5.0	+2%	
Fosc	Switching frequency			3.0		MHz
ILx	Maximum output current	2.9V≦Vin≦5.5V, Vout=1.2/1.5/1.8/3.3V	600			mA
		2.9V≦Vin≦5.5V, Vout=5V	300			
ILxlim	Limit current	2.9V≦Vin≦5.5V		2000		mA
Vpeak	Output transition response	Vin=5V, Vout=1.8V 10mA→100mA@ΔT=1μs			100	mV
Tr	Rising time	Vout=5V, Iout=0mA			2	ms
Tf	Falling time	Vout=5V, Iout=0mA			500	μs
Iss	Consumption current	Vin=5V, Iout=0mA		10		mA
VripO	Output ripple voltage	Vin=5V, Vout=1.8V, Iout=100mA		10		mV
η1	Efficiency peak	Vin=5V, Vout=1.2V Iout=0~600mA		73		%
		Vin=5V, Vout=1.5V Iout=0~600mA		77		%
		Vin=5V, Vout=1.8V Iout=0~600mA		82		%
		Vin=5V, Vout=3.3V Iout=0~600mA		90		%
		Vin=5V, Vout=5.0V Iout=0~600mA		- (full-on)		%

7. Clock Generator

7.1 Block Diagram

The following is a block diagram of the clock generator. The RD5T7319 has two PLLs.

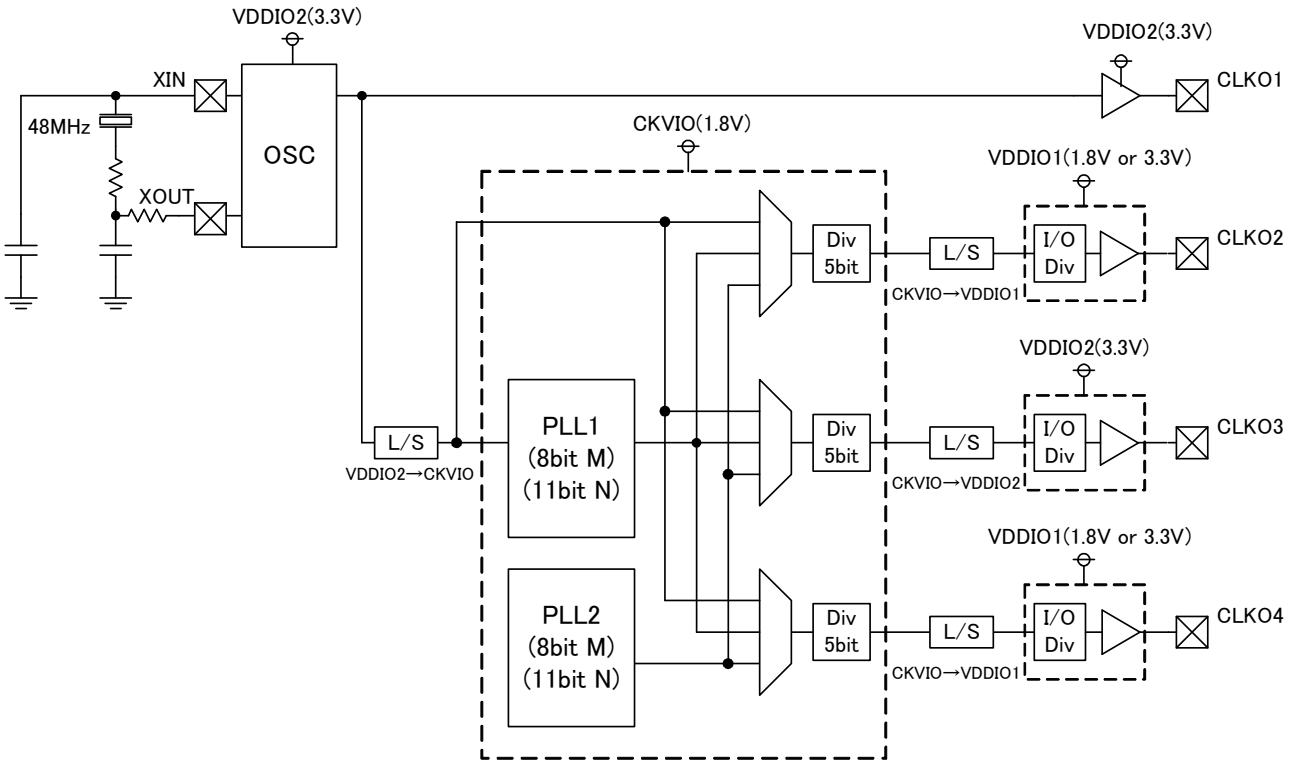


Fig. 7-1 Clock Generator block diagram

8. Real-Time Clock (RTC)

The RD5T7319 RTC has the following features;

- Time counters (counting hours, minutes, and seconds) and calendar counters (counting years, months, days, and weeks) (in BCD format)
- Interrupt circuit configured to generate interrupt signals (with interrupts ranging from 0.5 seconds to 1 month) to the CPU and provided with an interrupt flag and an interrupt halt
- 2 alarm interrupt circuits (Alarm_W for week, hour, and minute alarm settings and Alarm_D for hour and minute alarm settings)
- Built-in voltage detector
- With Power-on flag
- 32-kHz clock output pin (CMOS output.)
- Automatic identification of leap years up to the year 2099
- Selectable 12-hour and 24-hour mode settings
- High precision oscillation adjustment circuit

8.1 Block Diagram

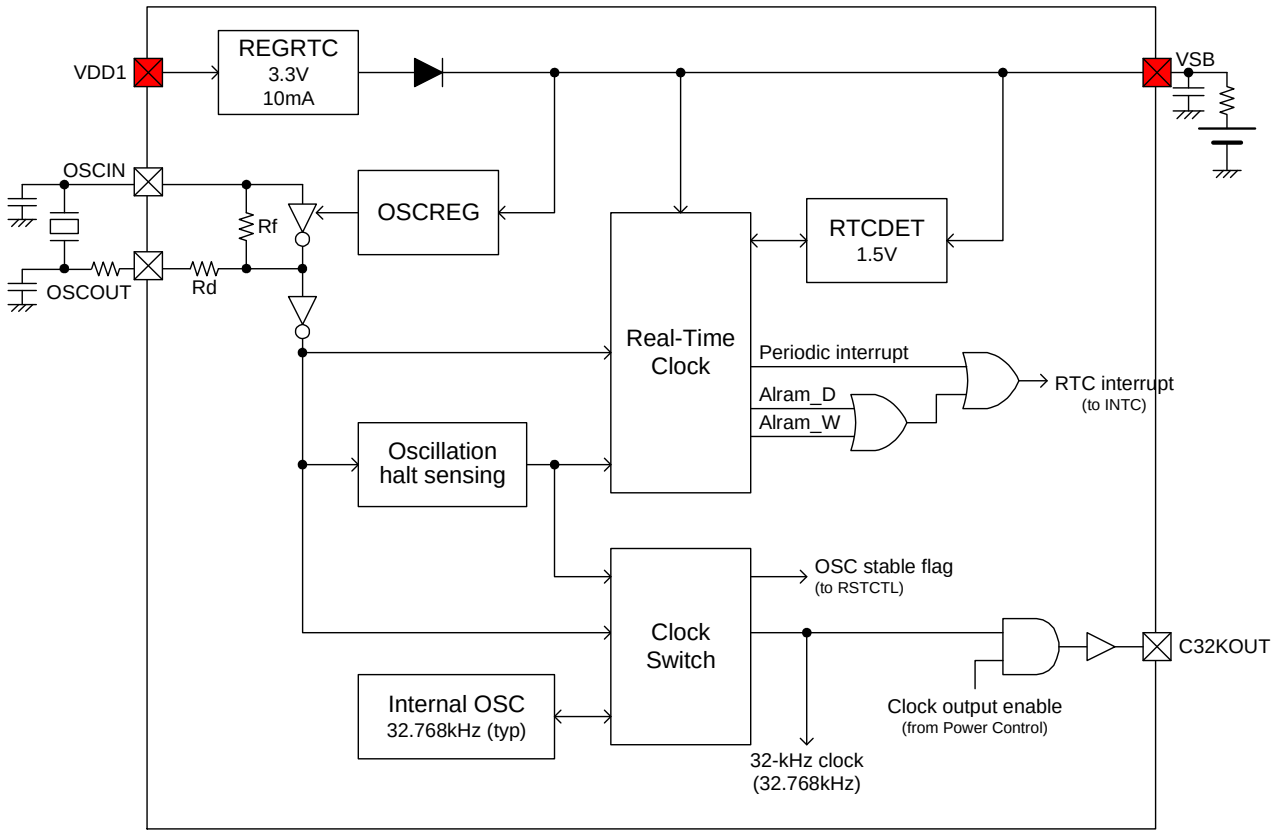


Fig. 8-1 Real-Time Clock Block Diagram

9. CPU Interface

The RD5T7319 uses I2C-Bus system for CPU connection through two wires. Connection and transfer system of I2C-Bus are described in the following sections.

9.1 I2C-Bus Operation

Within the procedure of I2C-Bus, unique situations arise which are defined as start and stop conditions.

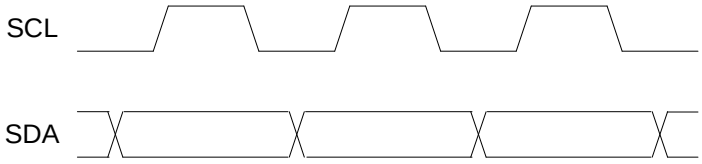


Fig. 9-1 I2C-Bus Data Transmission

A “H” to “L” transition on SDA line while SCL is “H” indicates a start condition. A “L” to “H” transition on SDA line while SCL is “H” defines a stop condition. Start and stop conditions are always generated by master. (Refer to the figure below). The bus is considered to be busy after start condition. The bus is considered to be free again a certain time after the stop condition.

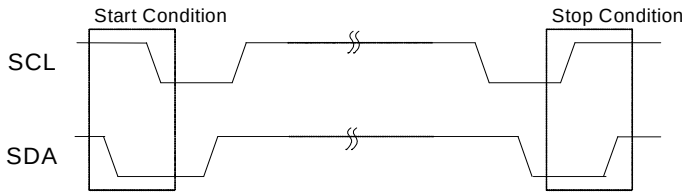


Fig. 9-2 I2C-Bus Start and Stop Condition

10. Electrical Characteristics

10.1 Absolute Maximum Ratings

The operation exceeding the below "Absolute Maximum Ratings" may cause not only permanent damage to the device, but also the reliability and safeness of its equipment. The operation of the device within the below stated ratings is not guaranteed.

Parameter	Symbol	Condition	Rated Value	Units
Power supply voltage	V_{IN}	VDD1, VINDD1, VINDD2, VINDD3, VINDD4	-0.3~6.5	V
	V_{DD}	VDDIO1, VDDIO2	-0.3~4.5	V
Signal input voltage range	V_{PIN}	EXTRSTB, LOWPWR	-0.3~5.8	V
		SEL1, SEL2	-0.3~VDD1+0.3	
		SCL, SDA	-0.3~5.8	
		XIN	-0.3~VDDIO2+0.3	
		OSCIN	-0.3~2.0	
Package allowable dissipation	PD	JEDEC substrate mounting state, Wind velocity 0m/s Ta=25°C Linear derating coefficient = 0.0178 W/°C	1780	mW
Storage temperature	T_{stg}	-----	-55~+125	degrees C

Table 10-1 Absolute Maximum Ratings

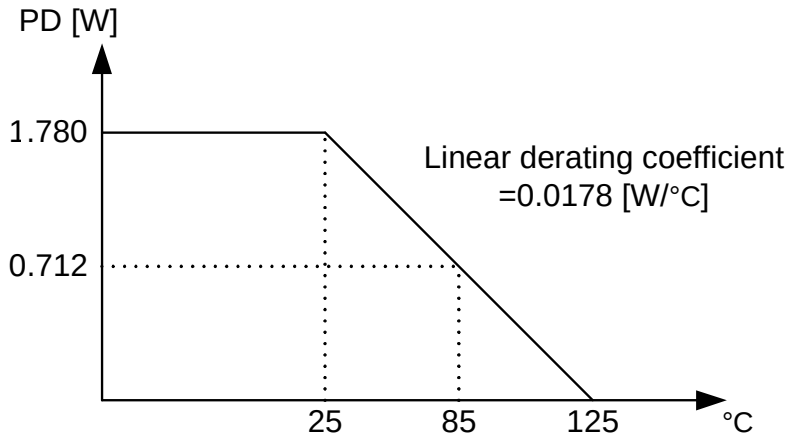


Fig. 10-1 Maximum Package Allowable Dissipation

10.2 Recommendation of Operating Conditions

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power supply voltage	V_{IN}	VDD1, VINDD1, VINDD2, VINDD3,VINDD4	2.9	5.0	5.5	V
	V_{DD1}	VDDIO1	1.7	3.3	3.6	V
	V_{DD2}	VDDIO2	3.0	3.3	3.6	V
Temperature of operation	T_a	-----	-30	-	+85	degrees C

Table 10-2 Recommendation of Operation Conditions

10.3 I/O Electrical Characteristics

10.3.1 VDD1 Interface

Open-drain output pin: RESETB, INTOUTB

Symbol	Parameter	Condition	MIN	TYP	MAX	Unit
VOL	“L” output voltage	IOL = 2mA	-	-	0.4	V
IOZ	Output leakage current at “OFF”	VI = 0~VDD1	-1	-	1	uA

CMOS Schmitt input pin: SEL1, SEL2

Symbol	Parameter	Condition	MIN	TYP	MAX	Unit
VIH	“H” input voltage (CMOS Schmitt)		VDD1 x0.8	-	VDD1 +0.3	V
VIL	”L” input voltage (CMOS Schmitt)		-	-	VDD1 x0.2	V
IIL	Input leakage current	VI = 0~VDD1	-1	-	1	uA

NMOS input pin: EXTRSTB, LOWPWR

Symbol	Parameter	Condition	MIN	TYP	MAX	Unit
VIH	“H” input voltage (NMOS)		1.4	-	5.5	V
VIL	”L” input voltage (NMOS)		-	-	0.4	V
IIL	Input leakage current	VI = 0~5.5V	-1	-	1	uA

10.3.2 VDDIO1 Interface

CMOS output1 pin: C32KOUT, L0DET

Symbol	Parameter	Condition	MIN	TYP	MAX	Unit
VOH	“H” output voltage	IOL = -4mA	VDDIO1 x0.8	-	-	V
VOL	“L” output voltage	IOL = 4mA	-	-	0.4	V

CMOS output2 pin: CLKO2, CLKO4

Symbol	Parameter	Condition	MIN	TYP	MAX	Unit
VOH	“H” output voltage	IOL = -4mA	VDDIO1 -0.5	-	-	V
VOL	“L” output voltage	IOL = 4mA	-	-	0.5	V

10.3.3 VDDIO2 Interface

CMOS Schmitt input/output pin (5.5V tolerant, Open-drain output): SDA

Symbol	Parameter	Condition	MIN	TYP	MAX	Unit
VIH	“H” input voltage (CMOS)		VDDIO2 x0.8	-	5.5	V
VIL	”L” input voltage (CMOS)		-	-	VDDIO2 x0.2	V
VOL	“L” output voltage	IOL = 3mA	-	-	0.4	V
IOZ	Output leakage current at “OFF”	VI = 0~5.5V	-3	-	3	uA

CMOS Schmitt input pins (5.5V tolerant): SCL

Symbol	Parameter	Condition	MIN	TYP	MAX	Unit
VIH	“H” input voltage (CMOS)		VDDIO2 x0.8	-	5.5	V
VIL	”L” input voltage (CMOS)		-	-	VDDIO2 x0.2	V
IIL	Input leakage current	VI = 0~5.5V	-1	-	1	uA

CMOS output pin: CLKO1, CLKO3

Symbol	Parameter	Condition	MIN	TYP	MAX	Unit
VOH	“H” output voltage	IOL = -4mA	VDDIO2 -0.5	-	-	V
VOL	“L” output voltage	IOL = 4mA	-	-	0.5	V

10.4 Consumption Current

Operating Conditions (unless otherwise specified) Ta = 25℃, No-load

Parameter	Symbol	Condition	Min	Typ	Max	Units
Backup	V_{BK}	VDD1, VINDD1, VINDD2, VINDD3, VINDD4, VDDIO1, VDDIO2 = no power VSB = 3.3V	-	1.4	-	uA
Standby	V_{ST}	SEL1,2 = L/L, LOWPWR = High, VDD1, VINDD1, VINDD2, VINDD3, VINDD4 = 5.0V, VDDIO1 = 1.8V, VDDIO2 = 3.3V, DCDC1 = On (1.8V), DCDC2（ECOREG） = On (3.2V), DCDC3 = On (0.85V), DCDC4 = Off, CLKO1-4 = Disable, 48MHz-OSC = Disable	-	200	-	uA
Active	V_{AC}	SEL1,2 = L/L, LOWPWR = Low VDD1, VINDD1, VINDD2, VINDD3, VINDD4 = 5.0V, VDDIO1 = 1.8V (DCDC1 Output), VDDIO2 = 3.3V (DCDC2 Output), DCDC1 = On (1.8V), DCDC2 = On (3.3V), DCDC3 = On (1.15V), DCDC4 = Off, CLKO1 = Disable, CLKO2 = 24MHz, CLKO3 = 74.25MHz, CLKO4 = 11.2896MHz	-	30	-	mA

Table 10-3 Consumption Current

11. Revision History

DATE	Ver.	PAGE	ITEM	CHANGES
2012/09/19	1.00	First release		

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