POWER MANAGEMENT SYSTEM DEVICE

RC5T7315

Product Brief

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Electronic Devices Company

This specification is subject to change without notice.

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1. Outline

RC5T7315 is the Power management LSI that integrates Regulators, Battery Charger, and RTC in one chip.

2. Feature

■ Power Supplies
- 13 Linear Regulators
- Five Voltage Detectors (DET1, DETIO, DET2, UVLO, and SHDET)
- Reference Voltage Source
- 3ch Step-down DCDC Converters

■ Serial Interface

The interface circuit with CPU consists of 16-bit serial register (8-bit command and 8-bit address), the address decoder, and the transmitting register (8 bits).

■ GPIO

THIS BLOCK IS COMPOSED OF 14 I/O PINS WITH PULL-UP/DOWN CONTROL FUNCTION.

THE INPUT SIGNALS TO GPIO PINS ARE OUTPUT TO INTC BLOCK, AND THEY BECOME ONE OF THE INTERRUPT GENERATION FACTORS.

■ INTC Interrupt Controller (INTC)

INTC block detects the state change of external input signals (GPIO 14 bits) and the internal interrupt signals, and then it generates interrupt signals.

■ 10bit ADC

10bit ADC has 8-channel input ports with a multiplexer.

■ Battery Charger

-There are two external power supply input pins; VCHG1 and VCH2.
-When both VCHG1 and VCHG2 pins have a proper input of voltage range;
the priority is given to VCHG1 pin input. Proper voltage range: 4.0V < $V_{VCHG\ 1(VCHG2)}$ < 6.3V
-The efficient power supply to the system and battery is performed by the current limit protection and the charge current control.
-Various timers for the charge control are integrated.
-Chip temperature detection circuit is integrated, and it prevents the chip overheating due to the charge.
-Thermistor temperature monitoring circuit is integrated, and it stops charging at the detection of error temperature while charging. Also, the temperature can be monitored by the integrated ADC.
-LED connection pin is equipped; the external LED can be turned on。
-Maximum allowable current from VBAT pin to VSYS pin: 1.6A.
-VCHG1 and VCHG2 pin: 7V withstand (absolute maximum ratings)

■ Reset Control

The Reset Control circuit generates the RESETB signal by the 7 factors.

■ Real Time Clock

- The time and calendar data are transferred to CPU through serial transfer.
- Integrates the periodic interrupt circuit with alarm function
(RTC interrupt request can be output to INTOUT pin through INTC block).
- All the registers of integrated RTC have their own backup in BKBAT (REGRTC: always ON).

■ Package

CSP0606-120 (0.5mm pitch, PKG thickness = 1mm@MAX)

■ Process

CMOS 0.18μm

3. Block Diagram

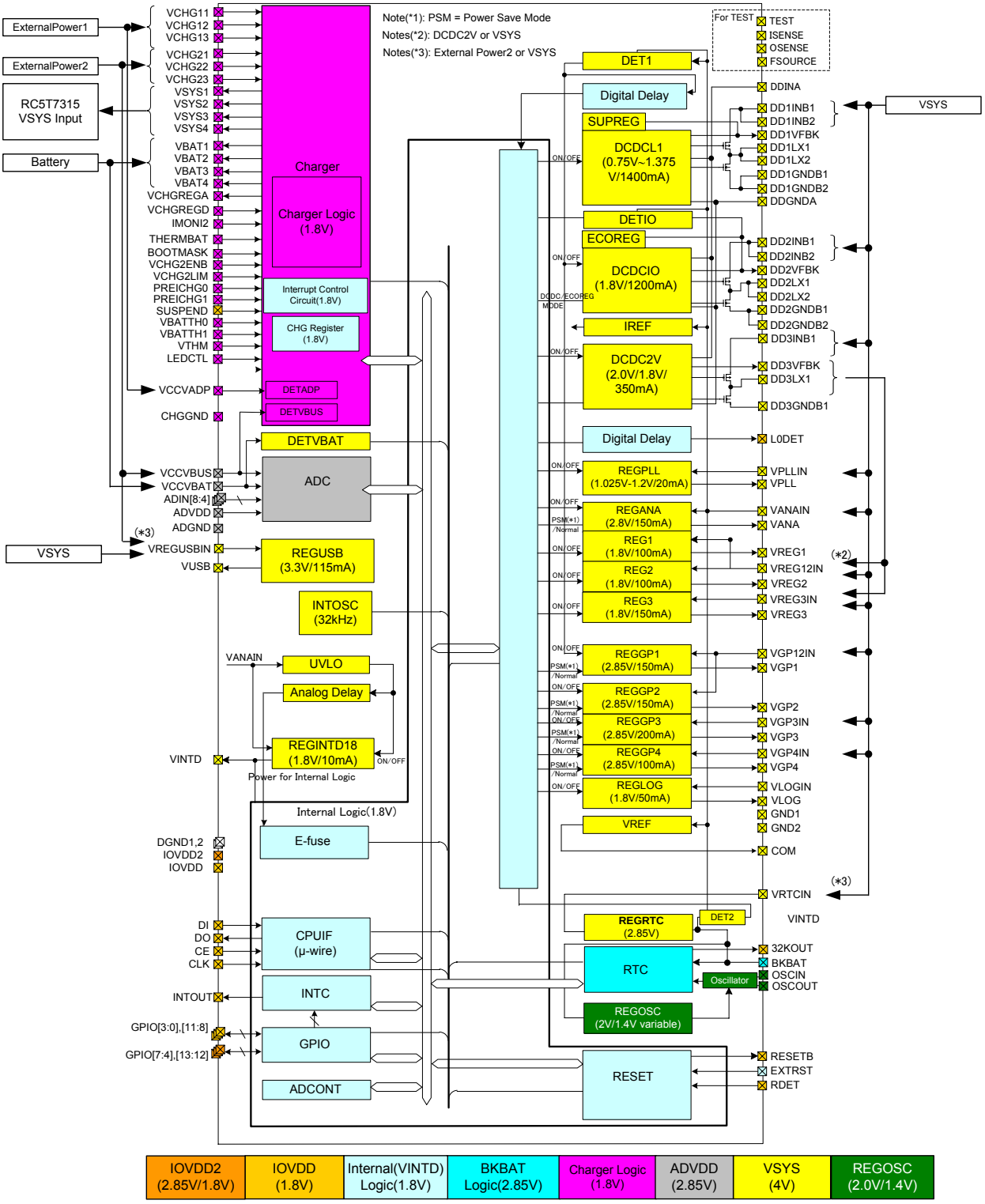


Fig 3-1 Block Diagram

4. Electrical Characteristics

4.1 Absolute Maximum Ratings

Exposure to the condition exceeded absolute maximum ratings may cause the permanent damages and affect the reliability and safety of both device and systems using the device. The functional operations cannot be guaranteed beyond specified values in the recommended conditions.

Parameter	Symbol	Condition	Rating	Units
Power voltage 1	VBAT1~3	Battery voltage pin	-0.3~7.0	V
Power voltage 2	ADVDD	2.85V/3.1V power supply pin	-0.3~4.5	V
Power voltage 3	IOVDD	1.8V power supply pin	-0.3~2.5	V
Power voltage 4	IOVDD2	1.8V/2.85V/3.1V power supply pin	-0.3~4.5	V
Power voltage 5	VBUS	5V power supply pin	-0.3~7.0	V
Power voltage 6	VCHG	CHG power supply pin	-0.3~7.0	V
Input voltage range	Vin	All input pins (VDD = VBAT, IOVDD, IOVDD2)	-0.3~VDD+0.3	V
Package power dissipation	PD	JEDEC substrate mounting state, wind velocity 0m/s, Ta=25°C Linear derating coefficient=0.0182 W/°C Power dissipation at Ta=85°C is given by: PD=(150-85)×(Linear derating coefficient)	2273	mW
Storage temperature	Tstg		-55 ~ +125	°C

Table 4-1 Absolute Maximum Ratings

4.2 Recommendation of Operating Conditions

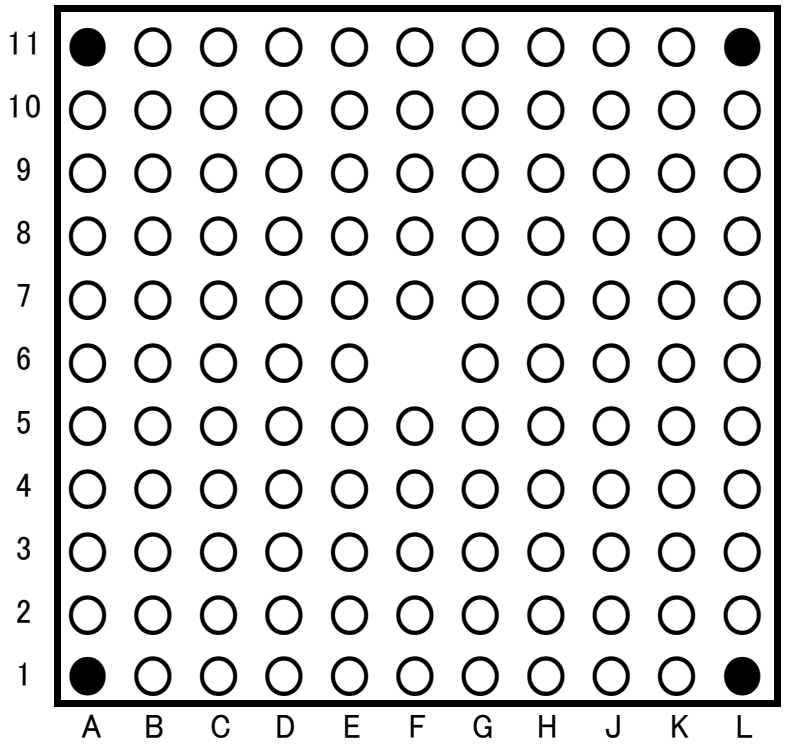
Parameter	Symbol	Condition	MIN	TYP	MAX	UNITS
Power voltage 1	VBAT1	VSYS connection power supply pin	3.1	3.6	5.5	V
	VBAT2	VSYS connection power supply pin	3.1	3.6	5.5	V
	VBAT3	DCDC2V/VSYS connection power supply pin	1.96	3.6	5.5	V
Power voltage 2	ADVDD	2.85V/3.1V power supply pin	2.75	2.85	3.25	V
Power voltage 3	IOVDD	1.8V power supply pin	1.7	1.8	1.9	V
Power voltage 4	IOVDD2	1.8V/2.85V/3.1V power supply pin	1.7	2.85	3.25	V
Power voltage 5	VBUS	5V power supply	4.5	5.0	5.5	V
Power voltage 6	VCHG	Charge power supply pin	4.5	5.0	5.5	V
Operating peripheral temperature	Ta	Temperature range that guarantees the described electrical characteristics	-30		+85	°C

Table 4-2 Recommendation of Operating Conditions

5. Pin Configuration

5.1 Pin Configuration

CSP0606 – 120 pin 0.5 mm pitch (TOP VIEW)



Pin Configuration (TOP VIEW)

	A	B	C	D	E	F	G	H	J	K	L
11	NC(OSENSE)	DD1INB1	DD1LX1	DD1GNDB1	DD2GNDB1	DD2LX1	DD2INB1	32KOUT	DO	DD3VFBK	NC(ISENSE)
10	GPIO4	DD1INB2	DD1LX2	DD1GNDB2	DD2GNDB2	DD2LX2	DD2INB2	RDET	CLK	DD3GNDB1	DD3LX1
9	GPIO5	DD1INA	DD1GNDA	DD1VFBK	DD2VFBK	NC(FSOURCE)	SUSPEND	RESETB	CE	EXTRST	DD3INB
8	GPIO11	IOVDD2	GPIO7	GPIO6	IOVDD	INTOUT	L0DET	DI	VINTD	VANA	VANAIN
7	VBATTH0	GPIO13	GPIO12	GPIO10	DGND2	DGND	GPIO9	GPIO1	COM	VGP2	VGP3
6	BOOTMASK	VBATTH1	LEDCTL	PREICHG1	PREICHG0		GPIO8	GPIO0	VGP3IN	VGP12IN	VGP1
5	VCHG11	IMONI2	VCHGREGA	VCHG2ENB	VCHG2LIM	GPIO3	GPIO2	GND1	VGP4IN	VGP4	OSCOUT
4	VCHG13	VCHG12	VCCVADP	CHGGND	ADGND	ADIN8	ADIN5	VREG3IN	GND2	BKBAT	OSCIN
3	VSYS4	VSYS3	VCCVBUS	VCHGREGD	ADVDD	ADIN6	ADIN4	VREG12IN	VLOGIN	VRTCIN	VLOG
2	VBAT3	VBAT4	VSYS2	VCHG21	VCHG22	VTHM	ADIN7	VUSB	VREG1	VPLLIN	VPLL
1	NC	VBAT1	VBAT2	VSYS1	VCHG23	THERMBAT	VCCVBAT	VREGUSBIN	VREG2	VREG3	NC(TEST)

Note*: Four pins at the corners of the device are “NC”.

Fig5-1 Pin Configuration

6. Pin Description

No.	Ball No.	Name	Block	Function	I/O	D/A	Type	PullUp/Down		I/F Voltage	Power	GND	Buff. State	Initial State	Note
								Up/Down	kΩ						
1	E9	DD2VFBK	DCDC	Feedback input/ECOREG output for Buck DCDCIO monitor	I	Analog	-	-	-	1.8V	DDINA	DDGNDA	-	-	
2	G11	DD2INB1	DCDC	Power pin for Buck DCDCIO buffer1	-	Power (VSYS:3.1～5.5V)	-	-	-	-	-	-	-	-	
3	G10	DD2INB2	DCDC	Power pin for Buck DCDCIO buffer2	-	Power (VSYS: 3.1～5.5V)	-	-	-	-	-	-	-	-	
4	F11	DD2LX1	DCDC	Buck DCDCIO LX1output pin	O	Analog	-	-	-	1.8V	DD2INB1,2	DD2GNDB1,2	-	-	
5	F10	DD2LX2	DCDC	Buck DCDCIO LX2 output pin	O	Analog	-	-	-	1.8V	DD2INB1,2	DD2GNDB1,2	-	-	
6	E11	DD2GNDB1	DCDC	Buck DCDCIO Buffer1 GND pin	-	GND	-	-	-	-	-	-	-	-	
7	E10	DD2GNDB2	DCDC	Buck DCDCIO Buffer2 GND pin	-	GND	-	-	-	-	-	-	-	-	
8	D11	DD1GNDB1	DCDC	Buck DCDCL1 Buffer1GND pin	-	GND	-	-	-	-	-	-	-	-	
9	D10	DD1GNDB2	DCDC	Buck DCDCL1 Buffer2 GND pin	-	GND	-	-	-	-	-	-	-	-	
10	C11	DD1LX1	DCDC	Buck DCDCL1 LX1 output pin	O	Analog	-	-	-	0.75V～1.375V	DD1INB1,2	DD1GNDB1,2	-	-	
11	C10	DD1LX2	DCDC	Buck DCDCL1 LX2 output pin	O	Analog	-	-	-	0.75V～1.375V	DD1INB1,2	DD1GNDB1,2	-	-	
12	B11	DD1INB1	DCDC	Buck DCDCL1 Buffer1 power pi	-	Power (VSYS:3.1～5.5V)	-	-	-	-	-	-	-	-	
13	B10	DD1INB2	DCDC	Buck DCDCL1 Buffer2 power pi	-	Power (VSYS:3.1～5.5V)	-	-	-	-	-	-	-	-	
14	C9	DDGNDA	DCDC	Common analog GND pin for Buck DCDC	-	GND	-	-	-	-	-	-	-	-	
15	B9	DDINA	DCDC	Common analog power pin for Buck DCDC	-	Power (VSYS:3.1～5.5V)	-	-	-	-	-	-	-	-	
16	D9	DD1VFBK	DCDC	Feedback input pin for Buck DCDCL1 monitor	I	Analog	-	-	-	0.75V～1.375V	DDINA	DDGNDA	-	-	
17	K10	DD3GNDB1	DCDC	Buck DCDC2V Buffer1 GND pin	-	GND	-	-	-	-	-	-	-	-	
18	L10	DD3LX1	DCDC	Buck DCDC2V LX1 output pin	O	Analog	-	-	-	2.0V/1.8V	DD3INB1	DD3GNDB1	-	-	
19	L9	DD3INB1	DCDC	Buck DCDC2V Buffer1 power p	-	Power (VSYS:3.1～5.5V)	-	-	-	-	-	-	-	-	
20	K11	DD3VFBK	DCDC	Feedback input pin for Buck DCDC2V monitor	I	Analog	-	-	-	2.0V/1.8V	DDINA	DDGNDA	-	-	
21	L4	OSCIN	RTC	Clock input of 32kHz Oscillation	I	Analog	-	-	-	1.4V/2.0V	OSCREG	GND1	-	-	
22	L5	OSCOUT	RTC	Clock output of 32kHz Oscillatio	O	Analog	-	-	-	1.4V/2.0V	OSCREG	GND1	-	-	
23	K2	VPLLIN	REG	REGPLL power pin	-	Power (VSYS:3.1～5.5V)	-	-	-	-	-	-	-	-	
24	L2	VPLL	REG	REGPLL output pin	O	Analog	-	-	-	1.025～1.2V	VPLLIN	GND2	-	-	
25	L8	VANAIN	REG	Power pin for REGANA/VREFL	-	Power (VSYS:3.1～5.5V)	-	-	-	-	-	-	-	-	
26	K8	VANA	REG	REGANA output pin	O	Analog	-	-	-	2.85V/3.1V	VANAIN	GND1	-	-	
27	J2	VREG1	REG	REG1output pin	O	Analog	-	-	-	1.8V	VREG12IN	GND2	-	-	
28	H3	VREG12IN	REG	Power pin for REG1/REG2	-	Power (VSYS:3.1～5.5V) or (DCDC2V:2.0V)	-	-	-	-	-	-	-	-	
29	J1	VREG2	REG	REG2 output pin	O	Analog	-	-	-	1.8V	VREG12IN	GND2	-	-	
30	J3	VLOGIN	REG	Power pin for REGLOG	-	Power (VSYS:3.1～5.5V)	-	-	-	-	-	-	-	-	

Table 6-1 Pin Description (1)

Table 6-2 Pin Description (2)

No.	Ball No.	Name	Block	Function	I/O	D/A	Type	PullUp/Down		I/F Voltage	Power	GND	Buff. State	Initial State	Note
								Up/Down	kΩ						
31	L3	VLOG	REG	REGLOG output pin	O	Analog	-	-	-	1.8V	VLOGIN	GND2	-	-	
32	K6	VGP12IN	REG	Power pin for REGGP1/REGGP2	-	Power (VSYS:3.1～5.5V)	-	-	-	-	-	-	-	-	
33	L6	VGP1	REG	REGGP1output pin	O	Analog	-	-	-	2.85V/3.1V	VGP12IN	GND1	-	-	
34	K7	VGP2	REG	REGGP2 output pin	O	Analog	-	-	-	2.85V/3.1V	VGP12IN	GND1	-	-	
35	J6	VGP3IN	REG	REGGP3 power pin	-	Power (VSYS:3.1～5.5V)	-	-	-	-	-	-	-	-	
36	L7	VGP3	REG	REGGP3 output pin	O	Analog	-	-	-	2.85V/3.1V	VGP3IN	GND1	-	-	
37	J5	VGP4IN	REG	REGGP4 power pin	-	Power (VSYS:3.1～5.5V)	-	-	-	-	-	-	-	-	
38	K5	VGP4	REG	REGGP4 output pin	O	Analog	-	-	-	2.85V/3.1V	VGP4IN	GND1	-	-	
39	H4	VREG3IN	REG	Power pin for REG3	-	Power (VSYS:3.1～5.5V) or (DCDC2V:2.0V)	-	-	-	-	-	-	-	-	
40	K1	VREG3	REG	REG3 output pin	O	Analog	-	-	-	1.8V	VREG3IN	GND2	-	-	
41	J7	COM	REG	Reference Voltage(VREF) output pin	O	Analog	-	-	-	2.0V	VANAIN	GND1	-	-	
42	H5	GND1	REG	GND pin for VREF/ REGANA/REGGP[1-4]/REGINTD	-	GND	-	-	-	-	-	-	-	-	
43	J4	GND2	REG	GND pin for REGRTC/ REGLOG/REGPLL/REG[1-3]	-	GND	-	-	-	-	-	-	-	-	
44	K3	VRTCIN	RTC	Power pin for REGRTC	-	Power (VSYS:3.1～5.5V)	-	-	-	-	-	-	-	-	
45	K4	BKBAT	RTC	REGRTC output pin/ RTC power pin	O	Analog/ Power(2.85V)	-	-	-	2.85V	VRTCIN	GND2	-	-	
46	A5	VCHG11	Charger	Charge Input1-1pin	-	Power (VCHG:4.5V～5.5V)	-	-	-	-	-	-	-	-	Connect to GND when not using Charger.
47	B4	VCHG12	Charger	Charge Input1-2 pin	-	Power (VCHG:4.5V～5.5V)	-	-	-	-	-	-	-	-	Connect to GND when not using Charger.
48	A4	VCHG13	Charger	Charge Input1-3 pin	-	Power (VCHG:4.5V～5.5V)	-	-	-	-	-	-	-	-	Connect to GND when not using Charger.
49	D2	VCHG21	Charger	Charge Input2-1 pin	-	Power (VBUS:4.5V～5.5V)	-	-	-	-	-	-	-	-	Connect to GND when not using Charger.
50	E2	VCHG22	Charger	Charge Input2-2 pin	-	Power (VBUS:4.5V～5.5V)	-	-	-	-	-	-	-	-	Connect to GND when not using Charger.
51	E1	VCHG23	Charger	Charge Input2-2 pin	-	Power (VBUS:4.5V～5.5V)	-	-	-	-	-	-	-	-	Connect to GND when not using Charger.
52	D1	VSYS1	Charger	System Power1 pin	-	Analog	-	-	-	-	-	CHGGND	-	-	Connect to GND when not using Charger.
53	C2	VSYS2	Charger	System Power2 pin	-	Analog	-	-	-	-	-	CHGGND	-	-	Connect to GND when not using Charger.
54	B3	VSYS3	Charger	System Power3 pin	-	Analog	-	-	-	-	-	CHGGND	-	-	Connect to GND when not using Charger.
55	A3	VSYS4	Charger	System Power4 pin	-	Analog	-	-	-	-	-	CHGGND	-	-	Connect to GND when not using Charger.
56	B1	VBAT1	Charger	Battery1 pin	-	Analog	-	-	-	-	-	CHGGND	-	-	Connect to GND when not using Charger.
57	C1	VBAT2	Charger	Battery2 pin	-	Analog	-	-	-	-	-	CHGGND	-	-	Connect to GND when not using Charger.
58	A2	VBAT3	Charger	Battery3 pin	-	Analog	-	-	-	-	-	CHGGND	-	-	Connect to GND when not using Charger.
59	B2	VBAT4	Charger	Battery4 pin	-	Analog	-	-	-	-	-	CHGGND	-	-	Connect to GND when not using Charger.
60	C5	VCHGREG	Charger	REG output pin/ Chage analog power pin	O	Analog/Power(2.5V	-	-	-	-	-	CHGGND	-	-	Connect to GND when not using Charger.

No.	Ball No.	Name	Block	Function	I/O	D/A	Type	PullUp/Down		I/F Voltage	Power	GND	Buff. State	Initial State	Note
								Up/Down	kΩ						
61	D3	VCHGREGD	Charger	REG output pin/ Carge digital power pin	O	Analog/Power(1.8V	-	-	-	-	-	CHGGND	-	-	Connect to GND when not using Charger.
62	B5	IMONI2	Charger	Output pin for Charge Current monitor	O	Analog	-	-	-	-	-	CHGGND	-	-	Connect to GND when not using Charger.
63	F1	THERMBAT	Charger	Battery temperature detection (Thermistor connection) pin	I	Analog	-	-	-	-	-	CHGGND	-	-	Connect to GND when not using Charger. But, connect with thermistor
64	D4	CHGGND	Charger	GND pin for Charger	-	GND	-	-	-	-	-	CHGGND	-	-	Connect to GND when not using Charger.
65	A6	BOOTMASK	Charger	System boot-up mask control p	I	Digital	CMOS Schmitt	Pull UP	1.1MΩ±50%	1.8V	VCHGREGD	DGND1,2	-	-	No connection when not using Charger.
66	D5	VCHG2ENB	Charger	Charger ON/OFF setting pin	I	Digital	CMOS Schmitt	Pull UP	1.1MΩ±50%	1.8V	VCHGREGD	DGND1,2	-	-	No connection when not using Charger.
67	E5	VCHG2LIM	Charger	VBUS current limit setting pin	I	Digital	CMOS Schmitt	Pull UP	1.1MΩ±50%	1.8V	VCHGREGD	DGND1,2	-	-	No connection when not using Charger.
68	E6	PREICHG0	Charger	Trickle charge current setting pi	I	Digital	CMOS Schmitt	Pull UP	1.1MΩ±50%	1.8V	VCHGREGD	DGND1,2	-	-	No connection when not using Charger.
69	D6	PREICHG1	Charger	Trickle charge current setting pi	I	Digital	CMOS Schmitt	Pull UP	1.1MΩ±50%	1.8V	VCHGREGD	DGND1,2	-	-	No connection when not using Charger.
70	G9	SUSPEND	Charger	Charge suspend setting pin	I	Digital	CMOS Schmitt	Pull DOWN	1.1MΩ±50%	1.8V	IOVDD	DGND1,2	-	-	No connection when not using Charger.
71	A7	VBATTH0	Charger	VSYS output ON/OFF threshold setting pin	I	Digital	CMOS Schmitt	Pull UP	1.1MΩ±50%	1.8V	VCHGREGD	DGND1,2	-	-	No connection when not using Charger.
72	B6	VBATTH1	Charger	VSYS output ON/OFF threshold setting pin	I	Digital	CMOS Schmitt	Pull UP	1.1MΩ±50%	1.8V	VCHGREGD	DGND1,2	-	-	No connection when not using Charger.
73	F2	VTHM	Charger	Voltage apply pin for battery temperature detection	I/O	Analog	-	-	-	-	VCHGREGA	CHGGND	-	-	No Connection when not using Charger. But, connect with thermistor
74	C6	LEDCTL	Charger	LED driver pin	O	Digital	O/D	-	-	-	VCHGREGD	DGND1,2	-	-	No connection when not using Charger.
75	C4	VCCVADP	Charger	VCCVADP detection	I	Power (VCHG:4.5V～5.5V)	-	-	-	-	VCHG1	CHGGND	-	-	No connection when not using Charger.
76	E4	ADGND	ADC	GND pin for AD converter	-	GND	-	-	-	-	-	-	-	-	
77	E3	ADVDD	ADC	Power pin for AD converter	-	Power (VGP1:2.85V)	-	-	-	-	-	-	-	-	
78	F4	ADIN8	ADC	AD converter input8 pin	I	Analog	-	-	-	0～2.85V	ADVDD	ADGND	-	-	No connection when not using Charger.
79	G2	ADIN7	ADC	AD cConverter input7 pin	I	Analog	-	-	-	0～2.85V	ADVDD	ADGND	-	-	No connection when not using Charger.
80	F3	ADIN6	ADC	AD converter input6 pin	I	Analog	-	-	-	0～2.85V	ADVDD	ADGND	-	-	No connection when not using Charger.
81	G4	ADIN5	ADC	AD converter input5 pin	I	Analog	-	-	-	0～2.85V	ADVDD	ADGND	-	-	No connection when not using Charger.
82	G3	ADIN4	ADC	AD converter input4 pin	I	Analog	-	-	-	0～2.85V	ADVDD	ADGND	-	-	No connection when not using Charger.
83	G1	VCCVBAT	ADC	ADC conversion BAT input / VCCVBAT detection	I	Power (VBAT:3.1V～4.5V)	-	-	-	0～4.5V	ADVDD	ADGND	-	-	
84	C3	VCCVBUS	ADC	ADC conversion VBUS input pin/VCCVBUS detection	I	Power (VBUS:4.5V～5.5V)	-	-	-	0～7V	ADVDD	ADGND	-	-	
85	H11	32KOUT	RTC	RTC clock output pin	O	Digital	CMOS	-	-	1.8V	IOVDD	DGND1,2	2mA	L	
86	H9	RESETB	RESET	Reset signal output pin	O	Digital	-	-	-	1.8V	IOVDD	DGND1,2	2mA	L	"H" output resistance (12kΩ±50%)
87	H10	RDET	RESET	Autonomous reset signal detection pin	I	Digital	CMOS Schmitt	-	-	1.8V	IOVDD	DGND1,2	-	-	
88	G8	L0DET	REGCONT	Output pin for Buck DCDCL1 boot-up	O	Digital	CMOS	-	-	1.8V	IOVDD	DGND1,2	2mA	L	
89	J11	DO	CPUIF	Serial data output pin	O	Digital	CMOS	-	-	1.8V	IOVDD	DGND1,2	8mA	Hi-Z	
90	H8	DI	CPUIF	Serial data input pin	I	Digital	CMOS Schmitt	-	-	1.8V	IOVDD	DGND1,2	-	-	

Table 6-3 Pin Description (3)

Table 6-4 Pin Description (4)

No.	Ball No.	Name	Block	Function	I/O	D/A	Type	PullUp/Down		I/F Voltage	Power	GND	Buff. State	Initial State	Note
								Up/Down	kΩ						
91	J9	CE	CPUIF	Chip selector pin	I	Digital	CMOS Schmitt	-	-	1.8V	IOVDD	DGND1,2	-	-	
92	J10	CLK	CPUIF	CLK for Serial data transmission/reception	I	Digital	CMOS Schmitt	-	-	1.8V	IOVDD	DGND1,2	-	-	
93	E7	DGND2	LOGIC	GND pin for IO/Internal logic	-	GND	-	-	-	-	-	-	-	-	
94	E8	IOVDD	LOGIC	Power pin for Internal IO	-	Power(DCDCIO: 1.8V)	-	-	-	-	-	-	-	-	
95	B8	IOVDD2	LOGIC	Power pin for Internal IO	-	Power (DCDCIO:1.8V) or	-	-	-	-	-	-	-	-	
96	B7	GPIO13	GPIO	GPIO13 input/output pin	I/O	Digital	CMOS Schmitt	Pull Up/Down (Register setting)	50kΩ±50%	1.8V/2.85V	IOVDD2	DGND1,2	2mA	"PullDpwn" IN	
97	C7	GPIO12	GPIO	GPIO12 input/output pin	I/O	Digital	CMOS Schmitt	Pull Up/Down (Register setting)	50kΩ±50%	1.8V/2.85V	IOVDD2	DGND1,2	2mA	"PullDpwn" IN	
98	A8	GPIO11	GPIO	GPIO11 input/output pin	I/O	Digital	CMOS Schmitt	Pull Up/Down (Register setting)	50kΩ±50%	1.8V/2.85V	IOVDD2	DGND1,2	2mA	"PullDpwn" IN	
99	D7	GPIO10	GPIO	GPIO10 input/output pin	I/O	Digital	CMOS Schmitt	Pull Up/Down (Register setting)	50kΩ±50%	1.8V/2.85V	IOVDD2	DGND1,2	2mA	"PullDpwn" IN	
100	G7	GPIO9	GPIO	GPIO9 input/output pin	I/O	Digital	CMOS Schmitt	Pull Up/Down (Register setting)	50kΩ±50%	1.8V	IOVDD	DGND1,2	2mA	"PullDpwn" IN	
101	G6	GPIO8	GPIO	GPIO8 input/output pin	I/O	Digital	CMOS Schmitt	Pull Up/Down (Register setting)	50kΩ±50%	1.8V	IOVDD	DGND1,2	2mA	"PullDpwn" IN	
102	C8	GPIO7	GPIO	GPIO7 input/output pin	I/O	Digital	CMOS Schmitt	Pull Up/Down (Register setting)	50kΩ±50%	1.8V/2.85V	IOVDD2	DGND1,2	2mA	"OPEN" IN	
103	D8	GPIO6	GPIO	GPIO6 input/output pin	I/O	Digital	CMOS Schmitt	Pull Up/Down (Register setting)	50kΩ±50%	1.8V/2.85V	IOVDD2	DGND1,2	2mA	"OPEN" IN	
104	A9	GPIO5	GPIO	GPIO5 input/output pin	I/O	Digital	CMOS Schmitt	Pull Up/Down (Register setting)	50kΩ±50%	1.8V/2.85V	IOVDD2	DGND1,2	2mA	"OPEN" IN	
105	A10	GPIO4	GPIO	GPIO4 input/output pin	I/O	Digital	CMOS Schmitt	Pull Up/Down (Register setting)	50kΩ±50%	1.8V/2.85V	IOVDD2	DGND1,2	2mA	"OPEN" IN	
106	F5	GPIO3	GPIO	GPIO3 input/output pin	I/O	Digital	CMOS Schmitt	Pull Up/Down (Register setting)	50kΩ±50%	1.8V	IOVDD	DGND1,2	2mA	"OPEN" IN	
107	G5	GPIO2	GPIO	GPIO2 input/output pin	I/O	Digital	CMOS Schmitt	Pull Up/Down (Register setting)	50kΩ±50%	1.8V	IOVDD	DGND1,2	2mA	"OPEN" IN	
108	H7	GPIO1	GPIO	GPIO1 input/output pin	I/O	Digital	CMOS Schmitt	Pull Up/Down (Register setting)	50kΩ±50%	1.8V	IOVDD	DGND1,2	2mA	"OPEN" IN	
109	H6	GPIO0	GPIO	GPIO0 input/output pin	I/O	Digital	CMOS Schmitt	Pull Up/Down (Register setting)	50kΩ±50%	1.8V	IOVDD	DGND1,2	2mA	"OPEN" IN	
110	F8	INTOUT	INTC	Interfupt output pin	O	Digital	CMOS	-	-	1.8V	IOVDD	DGND1,2	2mA	L	
111	K9	EXTRST	RESET	External reset signal detection p	I	Digital	CMOS Schmitt	Pull UP	100kΩ±50%	1.8V	VINTD	DGND1,2	-	-	
112	F7	DGND	LOGIC	GND pin for IO/Internal logic	-	GND	-	-	-	-	-	-	-	-	
113	H2	VUSB	REG	REGUSB output pin	O	Analog	-	-	-	3.3V	VREGUSBI	GND2	—	-	
114	H1	VREGUSBI	REG	REGUSB power pin	—	Power (VSYS:3.1～5.5V) or (VBUS:4.5～5.5V)	-	-	-	VSYS:3.1～5.5V VBUS:4.5～5.5V	-	-	—	-	
115	J8	VINTD	REG	REGINTD output pin/ Internal logic power	O	Analog/Power(1.8V)	-	-	-	1.8V	VANAIN	GND1	-	-	
116	L1	TEST	Test	TEST1 pin（Test mode control）	I	Digital	CMOS Schmitt	PullDown	1MΩ±50%	3.1～5.5V	VANAIN	DGND1,2	-	-	No connection or Connect to GND.
117	L11	ISENSE	Test	TEST2 pin（Test monitor）	I/O	Analog	-	-	-	3.1～5.5V	DDINA	DGND1,2	-	Hi-Z	No connection or Connect to GND.
118	A11	OSENSE	Test	TEST3 pin（Test monitor）	I/O	Analog	-	-	-	3.1～5.5V	DDINA	DGND1,2	-	Hi-Z	No connection or Connect to GND.
119	F9	FSOURCE	Test	TEST4 pin（E-Fuse write）	I/O	Analog	-	-	-	3.1～5.5V	-	DGND1,2	-	-	No connection or Connect to GND.
120	A1	NC	-	-	-	-	-	-	-	-	-	-	-	-	No connection or Connect to GND.

7. Power Control

7.1 Power Mode Control Transition Diagram

This is a reference example of the power mode control used in RC5T7315.
The relationship of each mode transition is shown in the figure below.

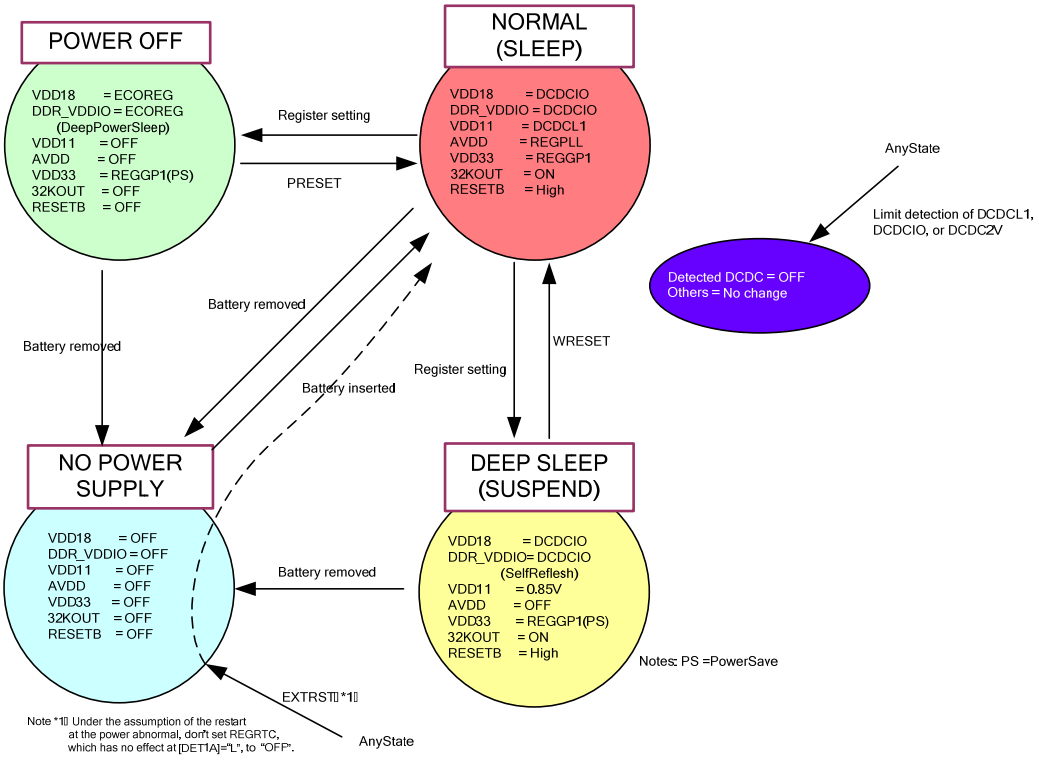


Fig 7-1 Power Mode Transition Diagram

7.2 Block Diagram

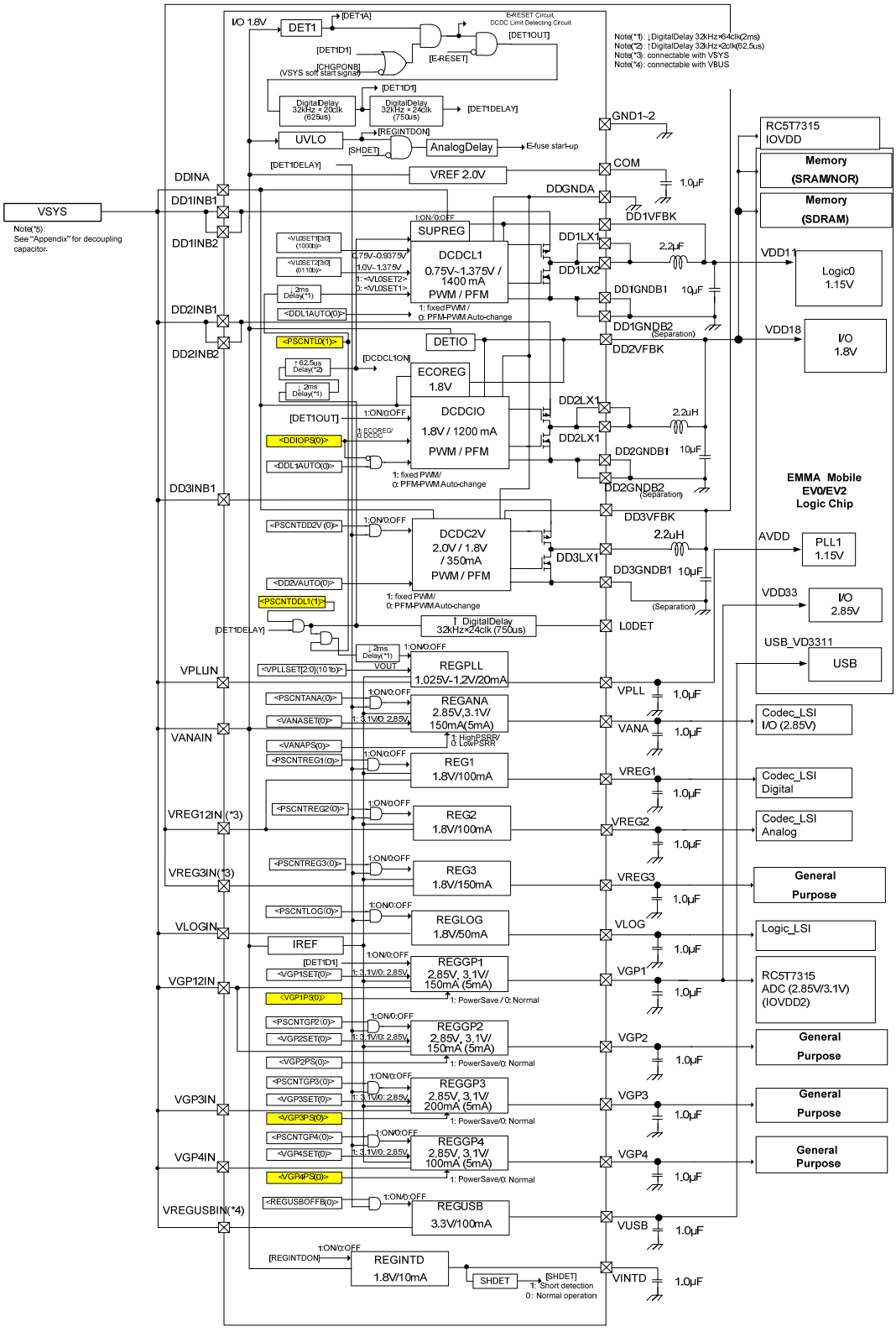


Fig 7-2 Power Block Diagram

8. Regulator

8.1 Regulators & DCDC Table

Table 8-1 Regulator & DCDC Table

No.	REG Name	Input Voltage(*1)	Output Voltage	Variable Voltage(PSM *2) or LowPSRR)	Maximum Output Current（PSM *2) or LowPSRR）	Consumption Current（PSM *2) or LowPSRR）	Transient Response 10μA～Iomax/2 Δt=1μs（PSM *2) or LowPSRR）	Ripple Rejection Rate（PSM *2) or LowPSRR）	Output Noise	Short-Circuit Current	Current Limit	Rising Time	ON/OFF Control	PSMz(*2)	Initial State	Capacitor	Comment
					MAX	TYP	MAX	TYP	TYP	MAX	MAX	MAX					
1	REGPLL	3.1V～5.5V	1.15V	1.025～1.2V Step 25mV 3bit	20mA	20uA	50mV	60dB@1kHz	100μVrms	100mA	150mA	250μs	Register control	-	ON	1.0μF	SinkTr built-in (SinkTr=OFF at DeepSleep)
2	REGLOG	3.1V～5.5V	1.8V	(1.7V～2.0V) *possible to trimming	50mA	3uA	100mV	50dB@120Hz	100μVrms	120mA	220mA	200μs	Register control	-	OFF	1.0μF	SinkTr built-in
3	REGANA	3.1V～5.5V	2.85V	2.85V/3.1V	150mA (5mA)	75uA (1uA)	50mV (100mV)	60dB@20kHz (40dB@120Hz)	55μVrms	150mA	350mA	200μs	Register control	Built-in	OFF	1.0μF	SinkTr built-in
4	REG1	1.96V～5.5V	1.8V	-	100mA	10uA	100mV	Vin=2.0V：40@1kHz Vin=3.6V：60@1kHz	300μVrms	190mA	270mA	200μs	Register control	-	OFF	1.0μF	SinkTr built-in
5	REG2	1.96V～5.5V	1.8V	-	100mA	100uA	100mV	Vin=2.0V：40dB@20kHz Vin=3.6V：70dB@20kHz	60μVrms	190mA	270mA	200μs	Register control	-	OFF	1.0μF	SinkTr built-in
6	REG3	1.96V～5.5V	1.8V	-	150mA	10uA	150mV	Vin=2.0V：30@1kHz Vin=3.6V：40@1kHz	300μVrms	190mA	300mA	200μs	Register control	-	OFF	1.0μF	SinkTr built-in
7	REGGP1	3.1V～5.5V	2.85V	2.85V/3.1V	150mA (5mA)	75uA (1uA)	40mV	75dB@1kHz	55μVrms	100mA	350mA	200μs	Always ON (at DET1release)	Built-in	ON	1.0μF	SinkTr built-in
8	REGGP2	3.1V～5.5V	2.85V	2.85V/3.1V	150mA (5mA)	75uA (1uA)	40mV	75dB@1kHz	55μVrms	150mA	350mA	200μs	Register control	Built-in	OFF	1.0μF	SinkTr built-in
9	REGGP3	3.1V～5.5V	2.85V	2.85V/3.1V	200mA (5mA)	75uA (1uA)	60mV	75dB@1kHz	55μVrms	170mA	350mA	200μs	Register control	Built-in	OFF	1.0μF	SinkTr built-in
10	REGGP4	3.1V～5.5V	2.85V	2.85V/3.1V	100mA (5mA)	50uA (1uA)	60mV	70dB@1kHz	75μVrms	100mA	270mA	200μs	Register control	Built-in	OFF	1.0μF	SinkTr built-in
11	REGRTC	2.3V～5.5V	2.85V (2.2V at Vin=2.3V)	-	10mA	6uA	100mV	50db@1kHz	130μVrms	120mA	120mA	200μs	Always ON（at UVLO release）	-	ON	1.0μF	
12	REGUSB	4.35V～5.5V(VBUS) 3.3V～5.5V(VSYS)	3.3V	-	115mA (VBUS) 2mA (VSYS)	25uA	100mV (VBUS) 150mV (VSYS)	Vin=5.0V：65dB@1kHz Vin=3.6V：40dB@1kHz	110μVrms	150mA	230mA	200μs	Register control	-	OFF	1.0μF	
13	REGINTD	UVLO～5.5V	1.825V	-	10mA	1uA	-	-	-	30mA	30mA	-	Always ON（at UVLO release）	-	ON	1.0μF	SinkTr built-in

Notes(*1)：The condition of I/O potential difference ≧0.2V is necessary to be fulfilled.

Notes(*2)：PSM = Power Save Mode

No.	REG Name	Input Voltage	Output Voltage	Variable Voltage(V)	Maximum Output Current	Consumption Current（PFM）	Transient Response	Efficiency (PFM)	Output Ripple (PFM)	Current Limit	Rising Time	Oscillation Freq	ON/OFF Control	Initial State	Capacitor /L value	Comment
					MAX	TYP	MAX	TYP	TYP	TYP	MAX	TYP				
14	DCDCL1	3.1V～5.5V	1.15V	1.0～1.375V 25mV/step(Normal) 0.75～0.9375V 12.5mV/step（DeepSleep）	1400mA	200μA (50μA)	100mV	85%@100mA (82%@12mA / 82%@40mA)	10mV (25mV)	2000mA (2500mA by setting Register)	500μs	2.2MHz	Register control	ON	10μF (ceramic), 2.2μH	
15	DCDCIO	3.1V～5.5V	1.8V	-	1200mA	200μA (50μA)	100mV	88%@100mA (82%@2mA / 82%@10mA)	10mV (25mV)	1700mA	500μs	2.2MHz	Always ON(at DET1release)	ON	10μF (ceramic), 2.2μH	
16	DCDC2V	3.1V～5.5V	2.0V	2.0V/1.8V	350mA	200μA (50μA)	100mV	85%@100mA (82%@5.5mA / 82%@50mA)	10mV (25mV)	800mA	200μs	2.2MHz	Register control	OFF	10μF (ceramic), 2.2μH	

9. GPIO

This block is composed of 14 I/O pins with pull-up/down control function.
The input signals to GPIO pins are output to INTC block, and they become one of the interrupt generation factors.

9.1 Block Diagram

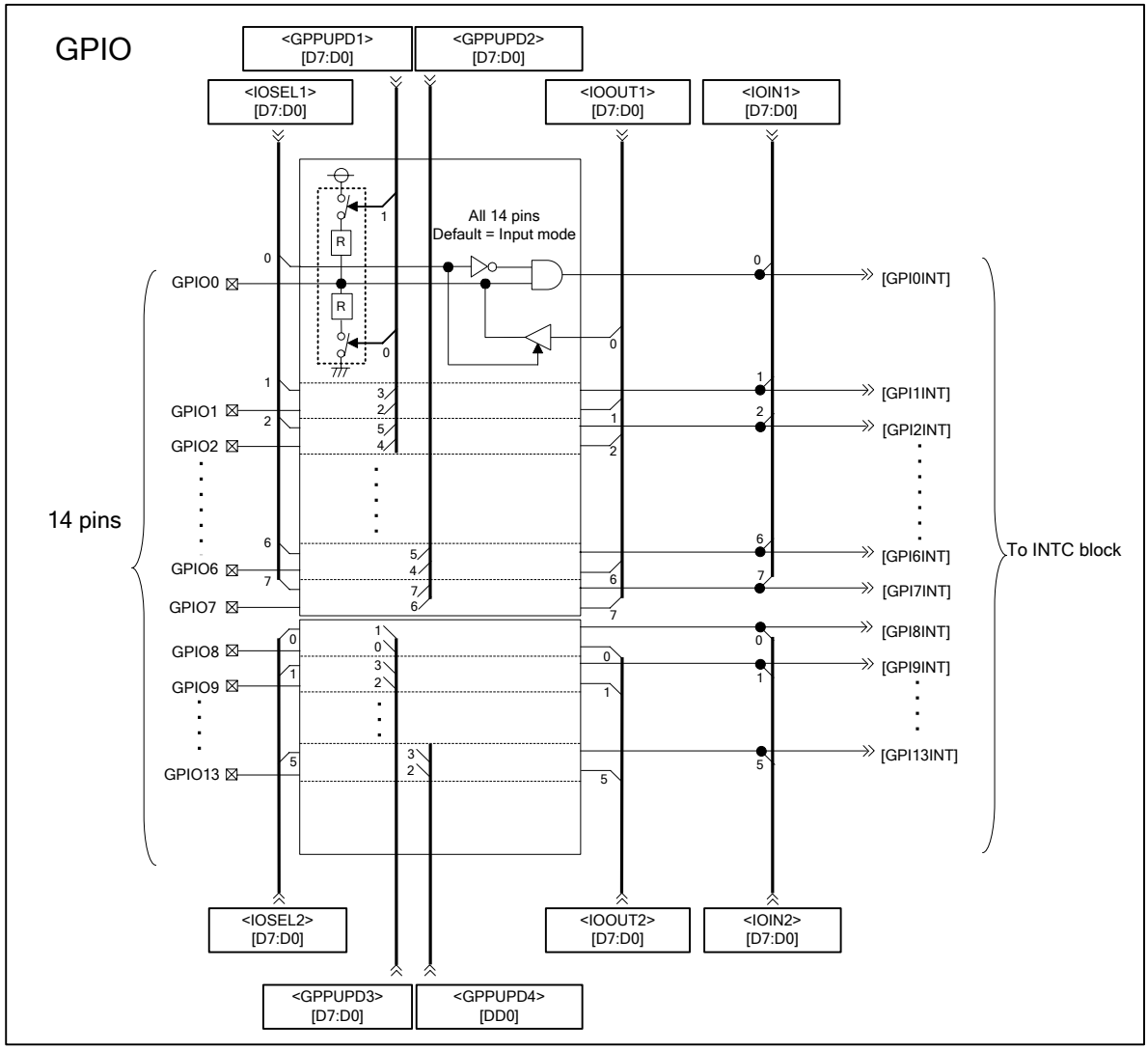


Fig 9-1 Block Diagram

Note*: Registers initialized by [RESET regC] (hardware reset): <IOSEL1~2> and <GPPUPD1~4>.
Registers initialized by [RESET regB] (internal reset): <IOIN1~2> and <IOOUT1~2>.

10. INTC

INTC block detects the state change of external input signals (GPIO 14 bits) and the internal interrupt signals, and then it generates interrupt signals. INTC block has the following functions; chattering rejection (30ms), forward interrupt mask, backward interrupt mask, and interrupt detecting type selection (level/rising edge/falling edge detection). The interrupt signal INTOUT, which is output from this block, continues to output “H” until the interrupt factor registers (<FACTOR1~3>) are cleared. To Wakeup (Warm Boost) from Deep Sleep/Suspend, INT_SIGNAL is used.

10.1 Block Diagram

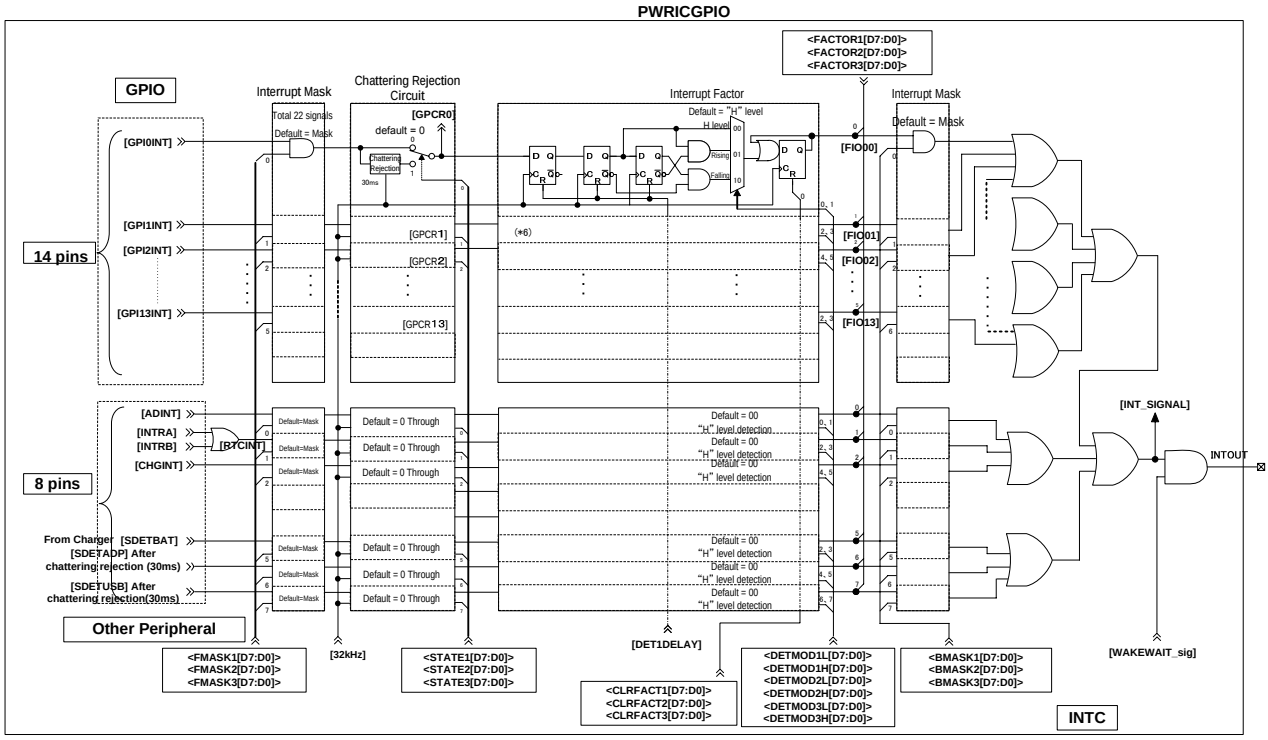
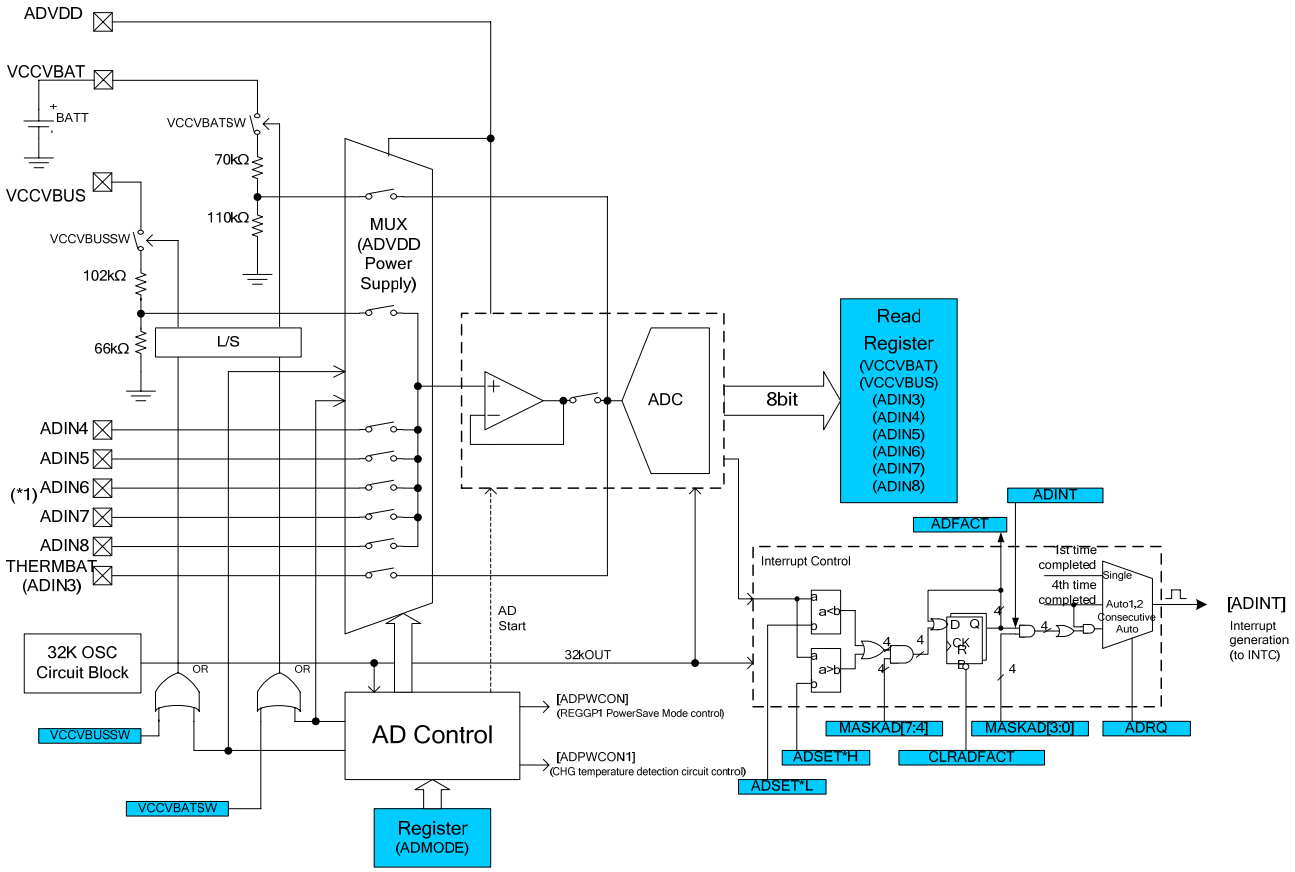


Fig 10-1 Block Diagram

11. ADC

1) Start ADC by the serial I/F register write.
2) The following two types of ADC can be selected:
   -Single ADC: Converts one input.
   -Auto ADC: Converts four inputs consecutively.
3) Automatically stops after completing the Single/Auto ADC.
4) VCCVBATSW/VCCVBUSSW automatic control function.
5) ADCLK frequency: 32kHz (OSC block).
6) ADC interval time (1s, 10s) is set, ADC is performed automatically, and interrupt signal is generated when ADC result is out of threshold value range.

11.1 Block Diagram



Note(*1): When unusing ADIN3-8, fix to N.C or a potential.

Fig 11-1 Block Diagram

12. Li-ion Battery Charger

RC5T7315 integrates Li-ion Battery charger, and the outline is as follows.

-There are two external power supply input pins; VCHG1 and VCH2.

-When both VCHG1 and VCHG2 pins have a proper input of voltage range;
the priority is given to VCHG1 pin input. Proper voltage range: 4.0V < $V_{VCHG\ 1(VCHG2)}$ < 6.3V

-The efficient power supply to the system and battery is performed by the current limit protection and the charge current control.

-Various timers for the charge control are integrated.

-Chip temperature detection circuit is integrated, and it prevents the chip overheating due to the charge.

-Thermistor temperature monitoring circuit is integrated, and it stops charging at the detection of error temperature while charging. Also, the temperature can be monitored by the integrated ADC (See “6-5.ADC” for details).

-The following charge modes are provided.

・VCHG1 charge: Charge while supplying power to the system. Start charging after automatically detecting the connection of external power supply (VCHG1).

・VCHG2 charge: Has following three modes.

a) Charge while supplying power to the system.

b) Battery voltage condition at power-on is changed depending on a level of BOOTMASK external pin.
When BOOTMASK = “H”, charging is started during the power supply to the system, and continues until the system’s power supply allowable voltage value set by VBATTH0 and VBATTH1. After that, the system turns on.
When BOOTMASK = “L”, the system can turn on if DET1 is released ([DET1] = “H”) at the connection with an external power.

c) In suspend state, the power is supplied from battery, and the charge operation turns OFF.

-There are pins that control the following: Trickle charge current, VCHG2 charge permission, VCHG2 current limit, power supply permission voltage to the system, VSYS output ON/OFF, and suspend.

-The followings are monitored, and interrupt signals are generated.

VCHG1 connection detection, VCHG2 connection detection, VCHG1 overvoltage, VCHG2 overvoltage
Battery connection detection, Battery overvoltage,
Timer completion (Trickle charge, Rapid charge)
During charge, complete charge
Thermistor high temperature detection, thermistor low temperature detection

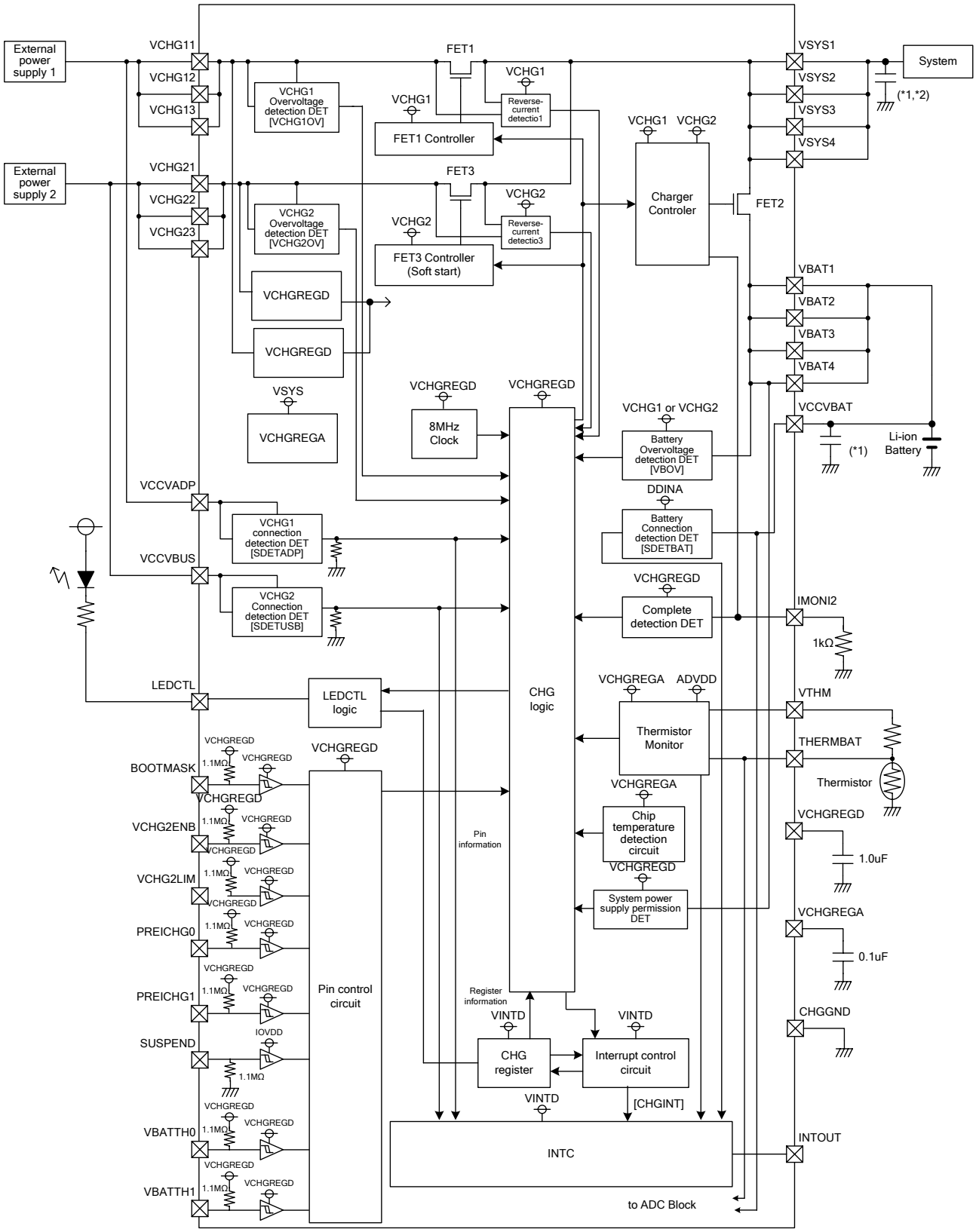
-Soft start circuit operates at the VCHG2 charge.

-LED connection pin is equipped; the external LED can be turned on。

-Maximum allowable current from VBAT pin to VSYS pin: 1.6A.

-VCHG1 and VCHG2 pin: 7V withstand (absolute maximum ratings)

12.1 Li-ion Battery Charger Block Diagram



Note(*1): See “Appendix” for decoupring capacitors of VCHG11/12/13 and VCHG21/22/23, and capacitors of VSYS1/2/3/4 and VBAT1/2/3/4/VCCVBAT.

Note(*2): The total of capacity connected with VSYS pin must become 50uF or less at the nominal capacity value.

Fig 12-1 Li-ion Battery Charger Block Diagram

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