

## Low Noise 150mA LDO REGULATOR

NO.EA-258-131024

### OUTLINE

The RP112x Series are CMOS-based voltage regulator (LDO) ICs, which have been developed using the CMOS process technology, with high output voltage accuracy, low-supply current, low On-resistance transistor, low noise output voltage and high ripple rejection. Each of the ICs is composed of the followings: a voltage reference unit, an error amplifier, a resistor-net for output voltage setting, a current limit circuit, and a chip enable circuit.

The RP112x features ultra low noise and its Ripple Rejection is as low as 80dB at  $f=1\text{kHz}$ , 75dB at  $f=10\text{kHz}$  and 65dB at  $f=100\text{kHz}$ . The Output Noise is also as low as Typ.  $10\mu\text{Vrms}$ . It is kept the low level at any Output Voltage. RP112x is suitable for the power source for the portable music player and RF module that demands for higher level of noise reduction. SOT-23-5 and SC-88A packages, a 1mm square DFN(PLP)1010-4 package are available.

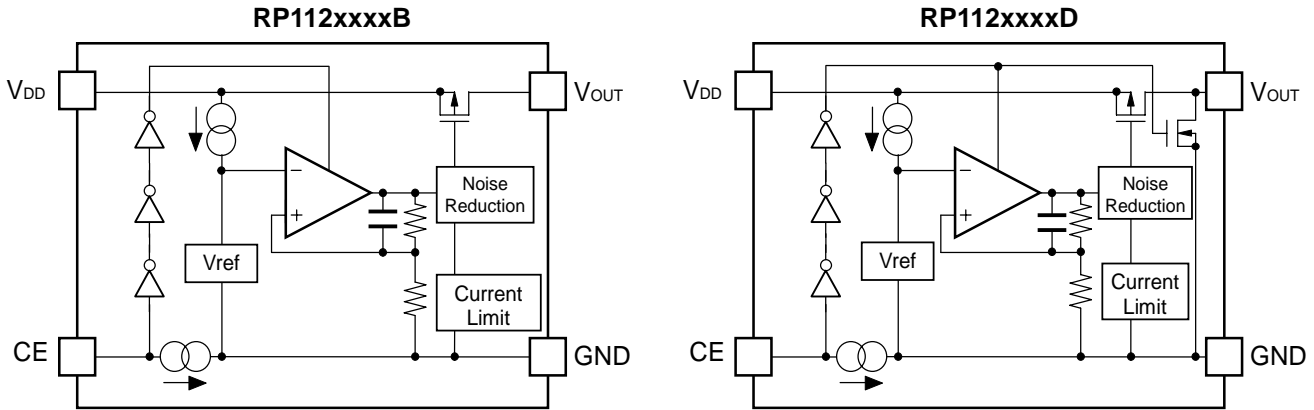
### FEATURES

- Supply Current ..... Typ.  $75\mu\text{A}$
- Standby Current ..... Typ.  $0.1\mu\text{A}$
- Dropout Voltage ..... Typ.  $0.20\text{V}$  ( $I_{\text{OUT}}=150\text{mA}$ ,  $V_{\text{OUT}}=2.8\text{V}$ )
- Ripple Rejection ..... Typ.  $80\text{dB}$  ( $f=1\text{kHz}$ )  
Typ.  $75\text{dB}$  ( $f=10\text{kHz}$ )  
Typ.  $65\text{dB}$  ( $f=100\text{kHz}$ )
- Output Voltage Accuracy .....  $\pm 1.0\%$
- Output Voltage Temperature Coefficient ..... Typ.  $\pm 30\text{ppm}/^\circ\text{C}$
- Line Regulation ..... Typ.  $0.02\%/V$
- Packages ..... DFN(PLP)1010-4, SC-88A, SOT-23-5
- Input Voltage Range .....  $2.0\text{V}$  to  $5.25\text{V}$
- Output Voltage Range .....  $1.2\text{V}$  to  $4.8\text{V}$  ( $0.1\text{V}$  steps)  
(For other voltages, please refer to MARK INFORMATION.)
- Short Current Limit ..... Typ.  $40\text{mA}$
- Built-in Foldback Protection Circuit
- Output Noise ..... Typ.  $10\mu\text{Vrms}$
- Ceramic capacitors are recommended to be used with this IC .....  $1.0\mu\text{F}$  or more

### APPLICATIONS

- Power source for portable communication equipment.
- Power source for electrical appliances such as cameras, VCRs and camcorders.
- Power source for battery-powered equipments.
- Power source for electrical home appliances.
- Power source for the portable music player
- Power source for RF module

## BLOCK DIAGRAMS



## SELECTION GUIDE

The output voltage, auto discharge function, package for the ICs can be selected at the user's request.

Product Name	Package	Quantity per Reel	Pb Free	Halogen Free
RP112Kxx1*-TR	DFN(PLP)1010-4	10,000 pcs	Yes	Yes
RP112Qxx2*-TR-FE	SC-88A	3,000 pcs	Yes	Yes
RP112Nxx1*-TR-FE	SOT-23-5	3,000 pcs	Yes	Yes

xx: Output voltage ( $V_{OUT}$ ) is selectable from 1.2V to 4.8V in 0.1V steps.

The second decimal point of the voltage is described as below.

1.25V: RP112x12x\*5

1.85V: RP112x18x\*5

2.85V: RP112x28x\*5

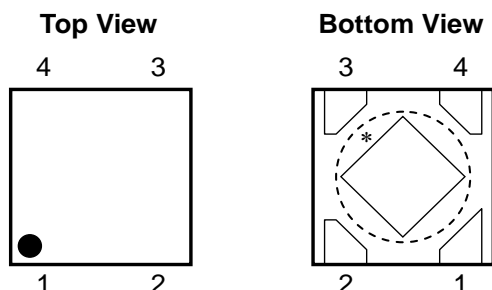
\*: Selections of CE pin polarity and Auto-discharge function are as shown below:

(B) CE pin polarity: "H" active, Auto-discharge function: No

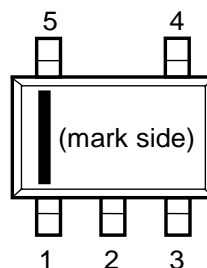
(D) CE pin polarity: "H" active, Auto-discharge function: Yes

## PIN CONFIGURATIONS

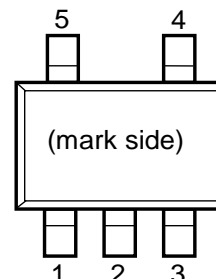
• DFN(PLP)1010-4



• SC-88A



• SOT-23-5



## PIN DESCRIPTIONS

• DFN(PLP)1010-4

Pin No.	Symbol	Description
1	$V_{OUT}$	Output Pin
2	GND	Ground Pin
3	CE	Chip Enable Pin ("H" Active)
4	$V_{DD}$	Input Pin

\*) Tab is GND level. (They are connected to the reverse side of this IC.)

The tab is better to be connected to the GND, but leaving it open is also acceptable.

• SC-88A

Pin No	Symbol	Pin Description
1	$V_{DD}$	Input Pin
2	GND	Ground Pin
3	CE	Chip Enable Pin ("H" Active)
4	NC	No Connection
5	$V_{OUT}$	Output Pin

• SOT-23-5

Pin No	Symbol	Pin Description
1	$V_{DD}$	Input Pin
2	GND	Ground Pin
3	CE	Chip Enable Pin ("H" Active)
4	NC	No Connection
5	$V_{OUT}$	Output Pin

**ABSOLUTE MAXIMUM RATINGS**

Symbol	Item	Rating	Unit
$V_{IN}$	Input Voltage	6.0	V
$V_{CE}$	Input Voltage (CE Pin)	6.0	V
$V_{OUT}$	Output Voltage	-0.3 to $V_{IN} + 0.3$	V
$I_{OUT}$	Output Current	180	mA
$P_D$	Power Dissipation (DFN(PLP)1010-4)*	400	mW
	Power Dissipation (SC-88A)*	380	
	Power Dissipation (SOT-23-5)*	420	
$T_{opt}$	Operating Temperature Range	-40 to 85	°C
$T_{stg}$	Storage Temperature Range	-55 to 125	°C

\*) For Power Dissipation, please refer to PACKAGE INFORMATION.

**ABSOLUTE MAXIMUM RATINGS**

Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause the permanent damages and may degrade the life time and safety for both device and system using the device in the field. The functional operation at or over these absolute maximum ratings is not assured.

## ELECTRICAL CHARACTERISTICS

Unless otherwise noted,  $V_{IN}=5.25V (V_{OUT} \geq 4.1V)$ ,  $V_{IN}=\text{Set } V_{OUT}+1.0V (1.5V < V_{OUT} < 4.1V)$ ,  
 $V_{IN}=2.5V (V_{OUT} \leq 1.5V)$ ,  $I_{OUT}=1mA$ ,  $C_{IN}=C_{OUT}=1.0\mu F$ .

The specifications surrounded by   are guaranteed by Design Engineering at  $-40^{\circ}C \leq T_a \leq 85^{\circ}C$ .

● RP112xxxxB/D

$T_a=25^{\circ}C$

Symbol	Item	Conditions	Min.	Typ.	Max.	Unit	
$V_{OUT}$	Output Voltage	$T_a=25^{\circ}C$	$V_{OUT} \geq 2.0V$	$\times 0.99$		$\times 1.01$	V
			$V_{OUT} < 2.0V$	-20		+20	mV
		$-40^{\circ}C \leq T_a \leq 85^{\circ}C$	$V_{OUT} \geq 2.0V$	<span style="border: 1px solid black; padding: 0 2px;">x0.985</span>		<span style="border: 1px solid black; padding: 0 2px;">x1.015</span>	V
			$V_{OUT} < 2.0V$	<span style="border: 1px solid black; padding: 0 2px;">-30</span>		<span style="border: 1px solid black; padding: 0 2px;">+30</span>	mV
$I_{OUT}$	Output Current		<span style="border: 1px solid black; padding: 0 2px;">150</span>			mA	
$\Delta V_{OUT}/\Delta I_{OUT}$	Load Regulation	$1mA \leq I_{OUT} \leq 150mA$	<span style="border: 1px solid black; padding: 0 2px;">-14</span>	0	<span style="border: 1px solid black; padding: 0 2px;">14</span>	mV	
$V_{DIF}$	Dropout Voltage	Please refer to "Dropout Voltage".					
$I_{SS}$	Supply Current	$I_{OUT}=0mA$	$V_{OUT} \geq 4.1V$		80	<span style="border: 1px solid black; padding: 0 2px;">100</span>	$\mu A$
			$V_{OUT} < 4.1V$		75		
$I_{standby}$	Standby Current	$V_{CE}=0V$		0.1	1.0	$\mu A$	
$\Delta V_{OUT}/\Delta V_{IN}$	Line Regulation	$\text{Set } V_{OUT}+0.3 \leq V_{IN} \leq 5.25V$	$V_{OUT} \geq 4.1V$		0.02	<span style="border: 1px solid black; padding: 0 2px;">0.10</span>	%V
		$\text{Set } V_{OUT}+0.5V \leq V_{IN} \leq 5.0V$	$1.7V \leq V_{OUT} \leq 4.1V$				
		$2.2V \leq V_{IN} \leq 5.0V$	$V_{OUT} < 1.7V$				
RR	Ripple Rejection	Ripple 0.2Vp-p, $I_{OUT}=30mA$ , $V_{IN}=5.25V$ ( $V_{OUT} \geq 4.1V$ ), $V_{IN}=\text{Set } V_{OUT}+1.0V$ ( $V_{OUT} < 4.1V$ )	$f=1kHz$		80		dB
			$f=10kHz$		75		
			$f=100kHz$		65		
$V_{IN}$	Input Voltage*		<span style="border: 1px solid black; padding: 0 2px;">2.0</span>		<span style="border: 1px solid black; padding: 0 2px;">5.25</span>	V	
$\Delta V_{OUT}/\Delta T_{opt}$	Output Voltage Temperature Coefficient	$-40^{\circ}C \leq T_a \leq 85^{\circ}C$		$\pm 30$		ppm/ $^{\circ}C$	
$I_{SC}$	Short Current Limit	$V_{OUT}=0V$		40		mA	
$I_{PD}$	CE Pull-down Current			0.3	<span style="border: 1px solid black; padding: 0 2px;">0.6</span>	$\mu A$	
$V_{CEH}$	CE Input Voltage "H"		<span style="border: 1px solid black; padding: 0 2px;">1.0</span>			V	
$V_{CEL}$	CE Input Voltage "L"				<span style="border: 1px solid black; padding: 0 2px;">0.4</span>	V	
en	Output Noise	$BW=10Hz \sim 100kHz$ , $I_{OUT}=30mA$		10		$\mu V_{rms}$	
$R_{LOW}$	Auto-discharge Nch Tr. ON Resistance (D version)	$V_{IN}=4.0V$ , $V_{CE}=0V$		60		$\Omega$	

All test categories were tested on the products under the pulse load condition ( $T_j \approx T_a=25^{\circ}C$ ) except Output Noise, Ripple Rejection, and Output Voltage Temperature Coefficient.

\*1) The maximum input voltage (Electrical Characteristics) is 5.25V. If, for any reason the maximum input voltage exceeds 5.25V, it has to be no more than 5.5V with 500hrs of the total operating time.

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**RP112x**

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NO.EA-258-131024

The specifications surrounded by   are guaranteed by Design Engineering at  $-40^{\circ}\text{C} \leq T_a \leq 85^{\circ}\text{C}$ .

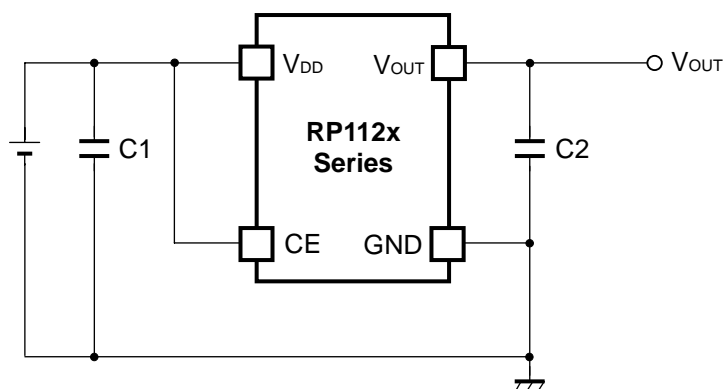
**• Dropout Voltage** $T_a=25^{\circ}\text{C}$ 

Output Voltage $V_{\text{OUT}}$ (V)	Dropout Voltage $V_{\text{DIF}}$ (V)		
	Condition	Typ.	Max.
$1.2\text{V} \leq V_{\text{OUT}} < 1.3\text{V}$	$I_{\text{OUT}}=150\text{mA}$	0.39	0.80
$1.3\text{V} \leq V_{\text{OUT}} < 1.4\text{V}$		0.37	0.70
$1.4\text{V} \leq V_{\text{OUT}} < 1.5\text{V}$		0.34	0.60
$1.5\text{V} \leq V_{\text{OUT}} < 1.7\text{V}$		0.32	0.50
$1.7\text{V} \leq V_{\text{OUT}} < 2.0\text{V}$		0.29	0.41
$2.0\text{V} \leq V_{\text{OUT}} < 2.5\text{V}$		0.25	0.36
$2.5\text{V} \leq V_{\text{OUT}} < 2.8\text{V}$		0.22	0.31
$2.8\text{V} \leq V_{\text{OUT}} \leq 4.8\text{V}$		0.20	0.28

**RECOMMENDED OPERATING CONDITIONS (ELECTRICAL CHARACTERISTICS)**

All of electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating conditions. The semiconductor devices cannot operate normally over the recommended operating conditions, even if when they are used over such conditions by momentary electronic noise or surge. And the semiconductor devices may receive serious damage when they continue to operate over the recommended operating conditions.

## TYPICAL APPLICATIONS



External Parts Example:

C1, C2: Ceramic Capacitor 1.0 $\mu$ F, Murata, GRM155B31A105KE15

## TECHNICAL NOTES

### Phase Compensation

In these ICs, phase compensation is made for securing stable operation even if the load current is varied. For this purpose, use a 1.0 $\mu$ F or more capacitor C2.

In case of using a tantalum capacitor, the output may be unstable due to inappropriate ESR. Therefore, the full range of operating conditions for the capacitor in the application should be considered.

### PCB Layout

The high impedances of V<sub>DD</sub> and GND could be a reason for the noise pickup and unstable operation. Therefore, it is imperative that the impedances of V<sub>DD</sub> and GND be the lowest possible. Also, place a 1.0 $\mu$ F or more capacitor (C1) between V<sub>DD</sub> pin and GND pin as close as possible to each other.

As for C2 output capacitor that is used for phase compensation, place it between V<sub>OUT</sub> pin and GND as close as possible to each other (Refer to TYPICAL APPLICATIONS).

## PACKAGE INFORMATION

### • Power Dissipation (DFN(PLP)1010-4)

Power Dissipation ( $P_D$ ) depends on conditions of mounting on board. This specification is based on the measurement at the conditions below:

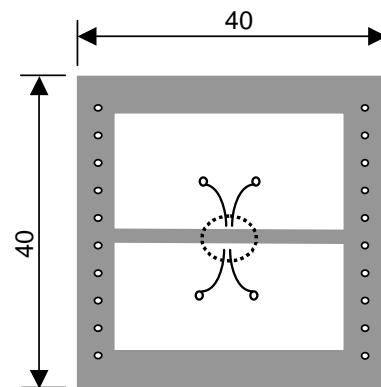
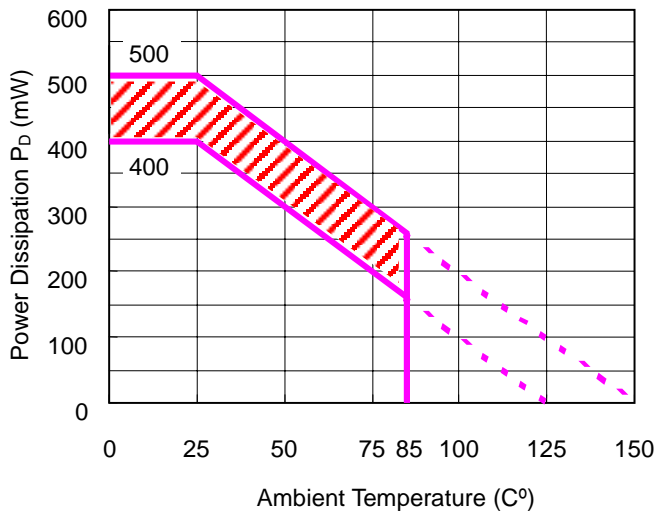
#### Measurement Conditions

	Standard Test land Pattern
Environment	Mounting on Board (Wind velocity=0m/s)
Board Material	Glass cloth epoxy plastic (Double sided)
Board Dimensions	40mm x 40mm x 1.6mm
Copper Ratio	Top side: Approx. 50%, Back side: Approx. 50%
Through-holes	$\phi$ 0.54mm x 24pcs

#### Measurement Result:

( $T_a=25^\circ\text{C}$ )

	Standard Test Land Pattern
Power Dissipation	400mW ( $T_{jmax}=125^\circ\text{C}$ ) 500mW ( $T_{jmax}=150^\circ\text{C}$ )
Thermal Resistance	$\theta_{ja}=(125-25^\circ\text{C})/0.4\text{W}=250^\circ\text{C/W}$ $\theta_{jc}=67^\circ\text{C/W}$



Measurement Board Pattern

IC Mount Area (Unit: mm)

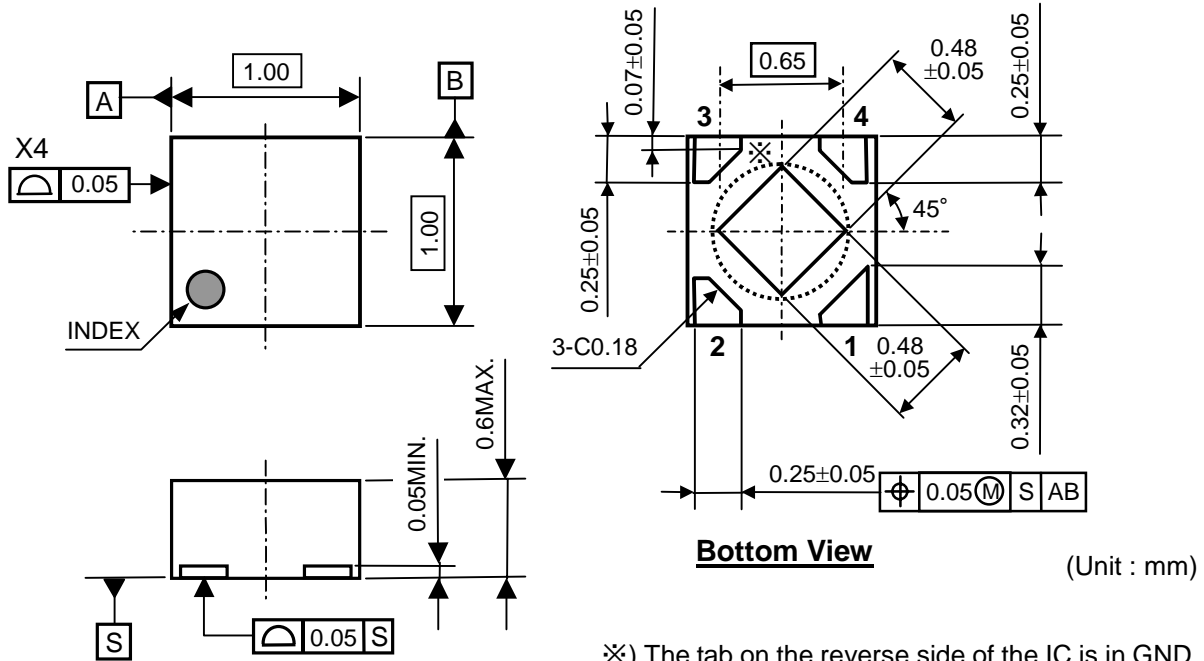
### Power Dissipation

The above graph shows that the power dissipation of the package under the conditions of  $T_{jmax}=125^\circ\text{C}$  and  $T_{jmax}=150^\circ\text{C}$ . The use under the diagonal line in the graph might have an affect on the ICs' lifetime. Please use the ICs within the limited operating time and estimated years as described below.

Operating Time	Estimated Years (4hrs/day)
13,000 hours	9 years



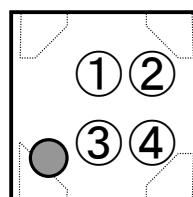
• Package Dimensions (DFN(PLP)1010-4)



※) The tab on the reverse side of the IC is in GND level. It should be connected to GND pin (recommended) or should be left open.

• Mark Specification (DFN(PLP)1010-4)

- ①②: Product Code ... Refer to "RP112K Series Mark Specification Table".
- ③④: Lot Number ... Alphanumeric Serial Number



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**RP112x**

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**• RP112K Series Mark Specification Table (DFN(PLP)1010-4)****RP112Kxx1B**

Product Name	①②	V <sub>SET</sub>
RP112K121B	1A	1.2V
RP112K131B	1C	1.3V
RP112K141B	1D	1.4V
RP112K151B	1E	1.5V
RP112K161B	1F	1.6V
RP112K171B	1G	1.7V
RP112K181B	1H	1.8V
RP112K191B	1K	1.9V
RP112K201B	1L	2.0V
RP112K211B	1M	2.1V
RP112K221B	1N	2.2V
RP112K231B	1P	2.3V
RP112K241B	1Q	2.4V
RP112K251B	1R	2.5V
RP112K261B	1S	2.6V
RP112K271B	1T	2.7V
RP112K281B	1U	2.8V
RP112K291B	1W	2.9V
RP112K301B	1X	3.0V
RP112K311B	1Y	3.1V
RP112K321B	1Z	3.2V
RP112K331B	2A	3.3V
RP112K341B	2B	3.4V
RP112K351B	2C	3.5V
RP112K361B	2D	3.6V
RP112K371B	2E	3.7V
RP112K381B	2F	3.8V
RP112K391B	2G	3.9V
RP112K401B	2H	4.0V
RP112K411B	2J	4.1V
RP112K421B	2K	4.2V
RP112K431B	2L	4.3V
RP112K441B	2M	4.4V
RP112K451B	2N	4.5V
RP112K461B	2P	4.6V
RP112K471B	2Q	4.7V
RP112K481B	2R	4.8V
RP112K121B5	1B	1.25V
RP112K181B5	1J	1.85V
RP112K281B5	1V	2.85V

**RP112Kxx1D**

Product Name	①②	V <sub>SET</sub>
RP112K121D	3A	1.2V
RP112K131D	3C	1.3V
RP112K141D	3D	1.4V
RP112K151D	3E	1.5V
RP112K161D	3F	1.6V
RP112K171D	3G	1.7V
RP112K181D	3H	1.8V
RP112K191D	3K	1.9V
RP112K201D	3L	2.0V
RP112K211D	3M	2.1V
RP112K221D	3N	2.2V
RP112K231D	3P	2.3V
RP112K241D	3Q	2.4V
RP112K251D	3R	2.5V
RP112K261D	3S	2.6V
RP112K271D	3T	2.7V
RP112K281D	3U	2.8V
RP112K291D	3W	2.9V
RP112K301D	3X	3.0V
RP112K311D	3Y	3.1V
RP112K321D	3Z	3.2V
RP112K331D	4A	3.3V
RP112K341D	4B	3.4V
RP112K351D	4C	3.5V
RP112K361D	4D	3.6V
RP112K371D	4E	3.7V
RP112K381D	4F	3.8V
RP112K391D	4G	3.9V
RP112K401D	4H	4.0V
RP112K411D	4J	4.1V
RP112K421D	4K	4.2V
RP112K431D	4L	4.3V
RP112K441D	4M	4.4V
RP112K451D	4N	4.5V
RP112K461D	4P	4.6V
RP112K471D	4Q	4.7V
RP112K481D	4R	4.8V
RP112K121D5	3B	1.25V
RP112K181D5	3J	1.85V
RP112K281D5	3V	2.85V

● **Power Dissipation (SC-88A)**

Power Dissipation ( $P_D$ ) depends on conditions of mounting on board. This specification is based on the measurement at the conditions below:

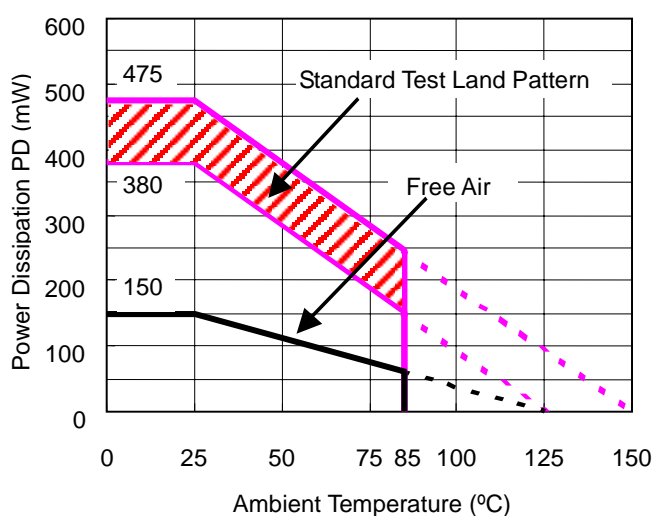
Measurement Conditions:

	<b>Standard Test Land Pattern</b>
Environment	Mounting on Board (Wind velocity=0m/s)
Board Material	Glass cloth epoxy plastic (Double Layers)
Board Dimensions	40mm × 40mm × 1.6mm
Copper Ratio	Top side: Approx. 50%, Back side: Approx. 50%
Through-hole	φ 0.5mm x 44pcs

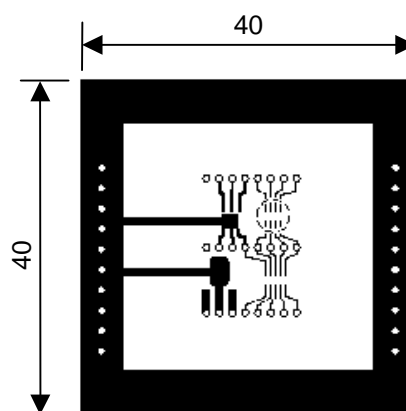
Measurement Result:

( $T_a=25^{\circ}\text{C}$ )

	<b>Standard Test Land Pattern</b>	<b>Free Air</b>
Power Dissipation	380mW ( $T_{jmax}=125^{\circ}\text{C}$ ) 475mW ( $T_{jmax}=150^{\circ}\text{C}$ )	150mW
Thermal Resistance	$\theta_{ja}=(125-25^{\circ}\text{C})/0.38\text{W}=263^{\circ}\text{C/W}$ $\theta_{jc}=75^{\circ}\text{C/W}$	$\theta_{ja}=(125-25^{\circ}\text{C})/0.15\text{W}=667^{\circ}\text{C/W}$ -



**Power Dissipation**



**Measurement Board Pattern**

○ IC Mount Area (Unit: mm)

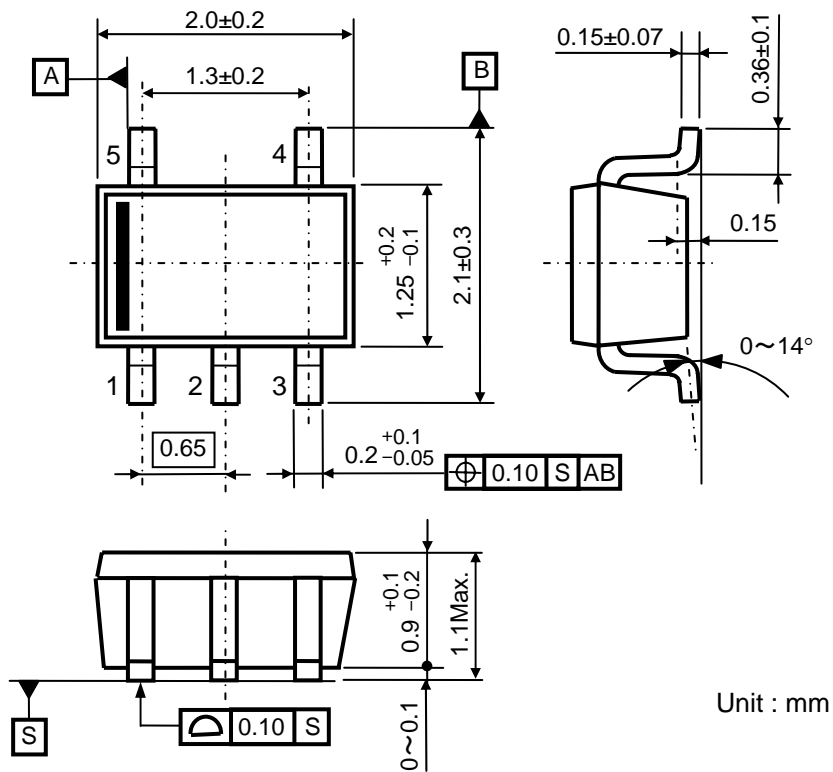
The above graph shows that the power dissipation of the package under the conditions of  $T_{jmax}=125^{\circ}\text{C}$  and  $T_{jmax}=150^{\circ}\text{C}$ . The use under the diagonal line in the graph might have an affect on the ICs' lifetime. Please use the ICs within the limited operating time and estimated years as described below.

Operating Time	Estimated Years (4hrs/day)
13,000 hours	9 years

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**RP112x**NO.EA-258-131024

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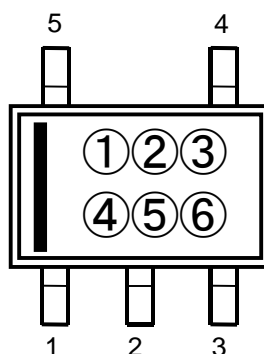
**• Package Dimensions (SC-88A)**

Unit : mm

**• Mark Specification (SC-88A)**

①②③④: Product Code ... Refer to "RP112Q Series Mark Specification Table".

⑤⑥ : Lot Number ... Alphanumeric Serial Number



● RP112Q Series Mark Specification Table (SC-88A)

RP112Qxx2B

Product Name	①②③④	V <sub>SET</sub>
RP112Q122B	AU12	1.2V
RP112Q132B	AU13	1.3V
RP112Q142B	AU14	1.4V
RP112Q152B	AU15	1.5V
RP112Q162B	AU16	1.6V
RP112Q172B	AU17	1.7V
RP112Q182B	AU18	1.8V
RP112Q192B	AU19	1.9V
RP112Q202B	AU20	2.0V
RP112Q212B	AU21	2.1V
RP112Q222B	AU22	2.2V
RP112Q232B	AU23	2.3V
RP112Q242B	AU24	2.4V
RP112Q252B	AU25	2.5V
RP112Q262B	AU26	2.6V
RP112Q272B	AU27	2.7V
RP112Q282B	AU28	2.8V
RP112Q292B	AU29	2.9V
RP112Q302B	AU30	3.0V
RP112Q312B	AU31	3.1V
RP112Q322B	AU32	3.2V
RP112Q332B	AU33	3.3V
RP112Q342B	AU34	3.4V
RP112Q352B	AU35	3.5V
RP112Q362B	AU36	3.6V
RP112Q372B	AU37	3.7V
RP112Q382B	AU38	3.8V
RP112Q392B	AU39	3.9V
RP112Q402B	AU40	4.0V
RP112Q412B	AU41	4.1V
RP112Q422B	AU42	4.2V
RP112Q432B	AU43	4.3V
RP112Q442B	AU44	4.4V
RP112Q452B	AU45	4.5V
RP112Q462B	AU46	4.6V
RP112Q472B	AU47	4.7V
RP112Q482B	AU48	4.8V
RP112Q122B5	AU01	1.25V
RP112Q182B5	AU02	1.85V
RP112Q282B5	AU03	2.85V

RP112Qxx2D

Product Name	①②③④	V <sub>SET</sub>
RP112Q122D	AV12	1.2V
RP112Q132D	AV13	1.3V
RP112Q142D	AV14	1.4V
RP112Q152D	AV15	1.5V
RP112Q162D	AV16	1.6V
RP112Q172D	AV17	1.7V
RP112Q182D	AV18	1.8V
RP112Q192D	AV19	1.9V
RP112Q202D	AV20	2.0V
RP112Q212D	AV21	2.1V
RP112Q222D	AV22	2.2V
RP112Q232D	AV23	2.3V
RP112Q242D	AV24	2.4V
RP112Q252D	AV25	2.5V
RP112Q262D	AV26	2.6V
RP112Q272D	AV27	2.7V
RP112Q282D	AV28	2.8V
RP112Q292D	AV29	2.9V
RP112Q302D	AV30	3.0V
RP112Q312D	AV31	3.1V
RP112Q322D	AV32	3.2V
RP112Q332D	AV33	3.3V
RP112Q342D	AV34	3.4V
RP112Q352D	AV35	3.5V
RP112Q362D	AV36	3.6V
RP112Q372D	AV37	3.7V
RP112Q382D	AV38	3.8V
RP112Q392D	AV39	3.9V
RP112Q402D	AV40	4.0V
RP112Q412D	AV41	4.1V
RP112Q422D	AV42	4.2V
RP112Q432D	AV43	4.3V
RP112Q442D	AV44	4.4V
RP112Q452D	AV45	4.5V
RP112Q462D	AV46	4.6V
RP112Q472D	AV47	4.7V
RP112Q482D	AV48	4.8V
RP112Q122D5	AV01	1.25V
RP112Q182D5	AV02	1.85V
RP112Q282D5	AV03	2.85V

# RP112x

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## • Power Dissipation (SOT-23-5)

Power Dissipation ( $P_D$ ) depends on conditions of mounting on board. This specification is based on the measurement at the conditions below:

(Power Dissipation (SOT-23-5) is a substitution of SOT-23-6.)

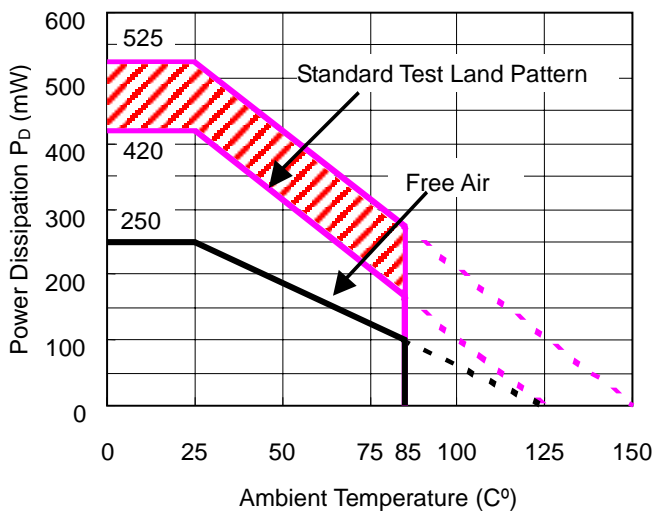
### Measurement Conditions

	Standard Test Land Pattern
Environment	Mounting on Board (Wind velocity=0m/s)
Board Material	Glass cloth epoxy plastic (Double sided)
Board Dimensions	40mm x 40mm x 1.6mm
Copper Ratio	Top side: Approx. 50%, Back side: Approx. 50%
Through-holes	$\phi$ 0.5mm x 44pcs

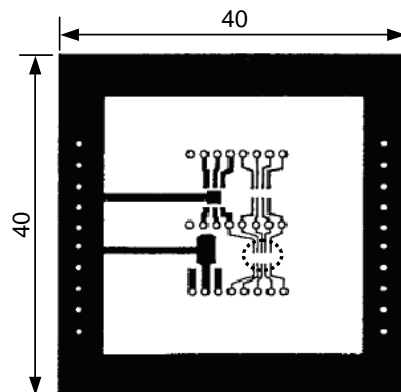
### Measurement Result:

( $T_a=25^\circ\text{C}$ )

	Standard Test Land Pattern	Free Air
Power Dissipation	420mW ( $T_{jmax}=125^\circ\text{C}$ ) 525mW ( $T_{jmax}=150^\circ\text{C}$ )	250mW ( $T_{jmax}=125^\circ\text{C}$ )
Thermal Resistance	$\theta_{ja}=(125-25^\circ\text{C})/0.42\text{W}=238^\circ\text{C/W}$	400 $^\circ\text{C/W}$



**Power Dissipation**



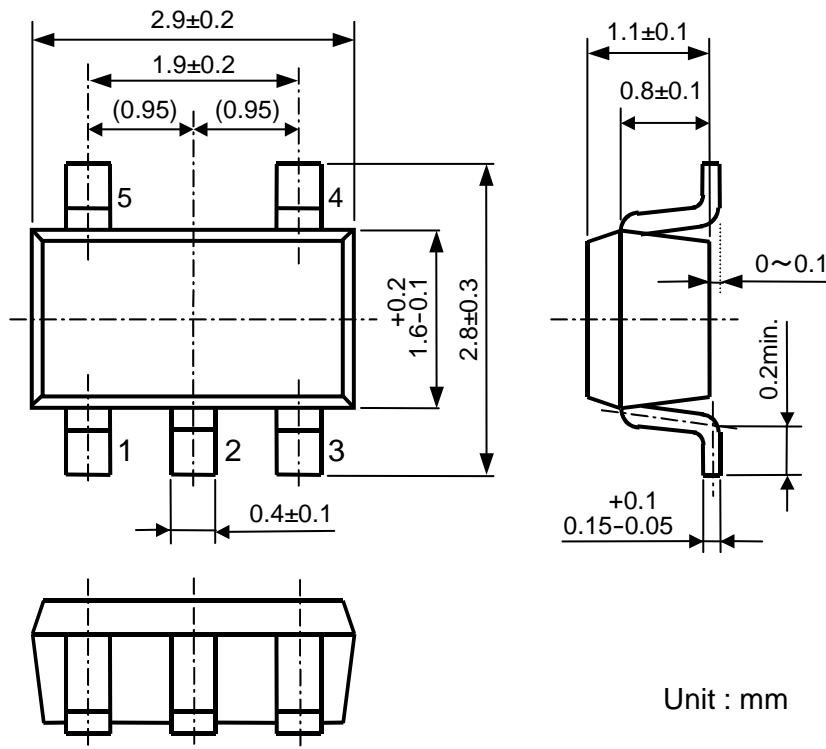
**Measurement Board Pattern**

○ IC Mount Area (Unit: mm)

The above graph shows that the power dissipation of the package under the conditions of  $T_{jmax}=125^\circ\text{C}$  and  $T_{jmax}=150^\circ\text{C}$ . The use under the diagonal line in the graph might have an affect on the ICs' lifetime. Please use the ICs within the limited operating time and estimated years as described below.

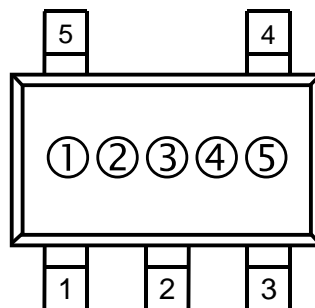
Operating Time	Estimated Years (4hrs/day)
13,000 hours	9 years

• Package Dimensions (SOT-23-5)



• Mark Specification (SOT-23-5)

- ①②③: Product Code ... Refer to "RP112N Series Mark Specification Table".
- ④⑤ : Lot Number ... Alphanumeric Serial Number



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**RP112x**

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**• RP112N Series Mark Specification Table (SOT-23-5)****RP112Nxx1B**

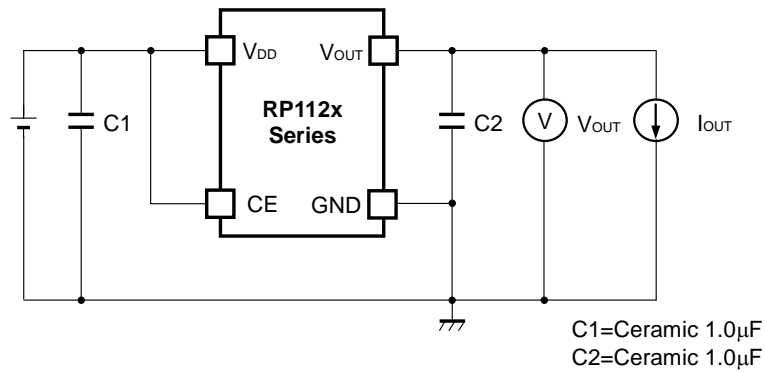
Product Name	①②③	V <sub>SET</sub>
RP112N121B	K12	1.2V
RP112N131B	K13	1.3V
RP112N141B	K14	1.4V
RP112N151B	K15	1.5V
RP112N161B	K16	1.6V
RP112N171B	K17	1.7V
RP112N181B	K18	1.8V
RP112N191B	K19	1.9V
RP112N201B	K20	2.0V
RP112N211B	K21	2.1V
RP112N221B	K22	2.2V
RP112N231B	K23	2.3V
RP112N241B	K24	2.4V
RP112N251B	K25	2.5V
RP112N261B	K26	2.6V
RP112N271B	K27	2.7V
RP112N281B	K28	2.8V
RP112N291B	K29	2.9V
RP112N301B	K30	3.0V
RP112N311B	K31	3.1V
RP112N321B	K32	3.2V
RP112N331B	K33	3.3V
RP112N341B	K34	3.4V
RP112N351B	K35	3.5V
RP112N361B	K36	3.6V
RP112N371B	K37	3.7V
RP112N381B	K38	3.8V
RP112N391B	K39	3.9V
RP112N401B	K40	4.0V
RP112N411B	K41	4.1V
RP112N421B	K42	4.2V
RP112N431B	K43	4.3V
RP112N441B	K44	4.4V
RP112N451B	K45	4.5V
RP112N461B	K46	4.6V
RP112N471B	K47	4.7V
RP112N481B	K48	4.8V
RP112N121B5	K01	1.25V
RP112N181B5	K02	1.85V
RP112N281B5	K03	2.85V

**RP112Nxx1D**

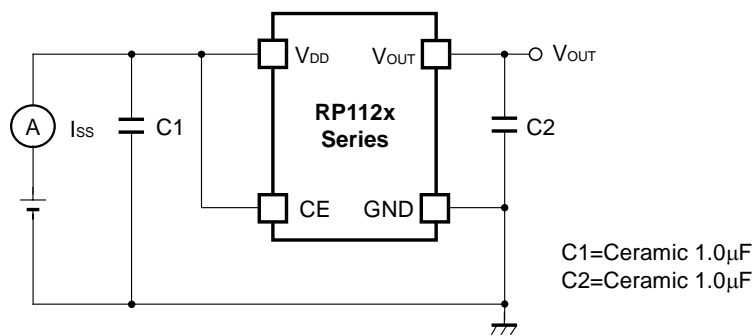
Product Name	①②③	V <sub>SET</sub>
RP112N121D	L12	1.2V
RP112N131D	L13	1.3V
RP112N141D	L14	1.4V
RP112N151D	L15	1.5V
RP112N161D	L16	1.6V
RP112N171D	L17	1.7V
RP112N181D	L18	1.8V
RP112N191D	L19	1.9V
RP112N201D	L20	2.0V
RP112N211D	L21	2.1V
RP112N221D	L22	2.2V
RP112N231D	L23	2.3V
RP112N241D	L24	2.4V
RP112N251D	L25	2.5V
RP112N261D	L26	2.6V
RP112N271D	L27	2.7V
RP112N281D	L28	2.8V
RP112N291D	L29	2.9V
RP112N301D	L30	3.0V
RP112N311D	L31	3.1V
RP112N321D	L32	3.2V
RP112N331D	L33	3.3V
RP112N341D	L34	3.4V
RP112N351D	L35	3.5V
RP112N361D	L36	3.6V
RP112N371D	L37	3.7V
RP112N381D	L38	3.8V
RP112N391D	L39	3.9V
RP112N401D	L40	4.0V
RP112N411D	L41	4.1V
RP112N421D	L42	4.2V
RP112N431D	L43	4.3V
RP112N441D	L44	4.4V
RP112N451D	L45	4.5V
RP112N461D	L46	4.6V
RP112N471D	L47	4.7V
RP112N481D	L48	4.8V
RP112N121D5	L01	1.25V
RP112N181D5	L02	1.85V
RP112N281D5	L03	2.85V



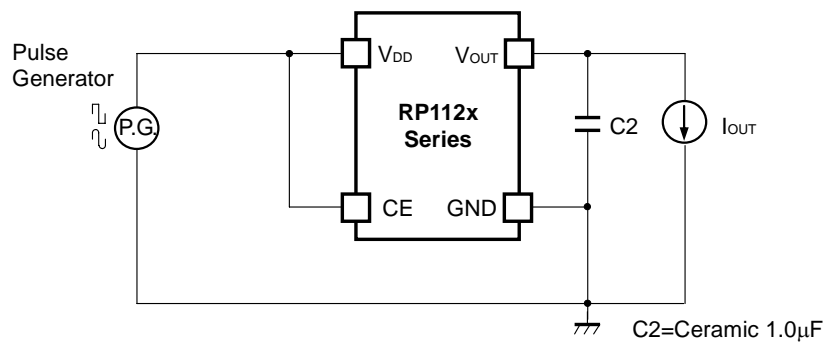
## TEST CIRCUIT



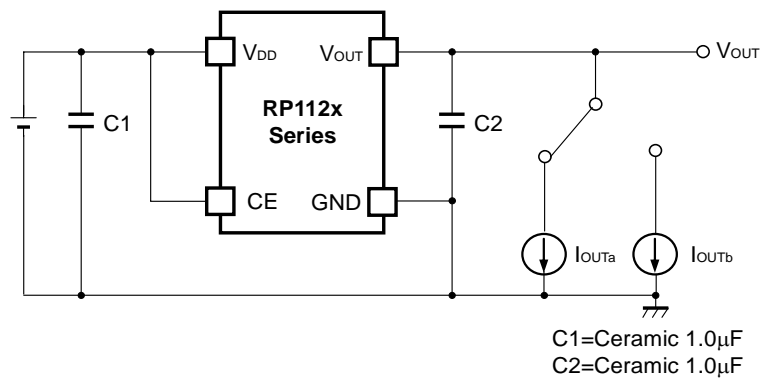
Basic Test Circuit



Test Circuit for Supply Current



Test Circuit for Ripple Rejection

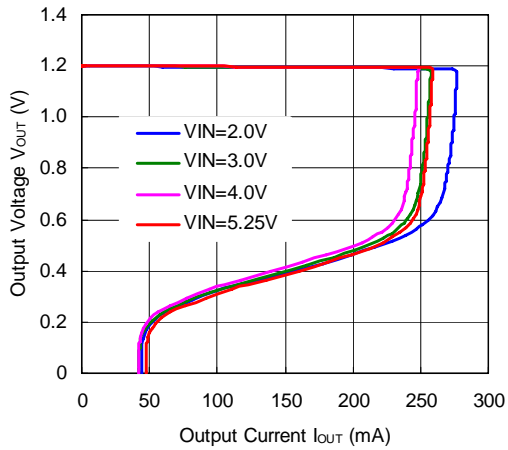


Test Circuit for Load Transient Response

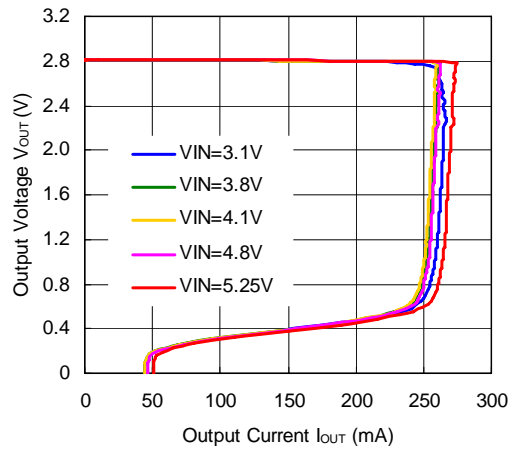
## Typical Characteristics

### 1) Output Voltage vs. Output Current (C1=Ceramic 1.0 $\mu$ F, C2=Ceramic 1.0 $\mu$ F, T<sub>opt</sub>=25°C)

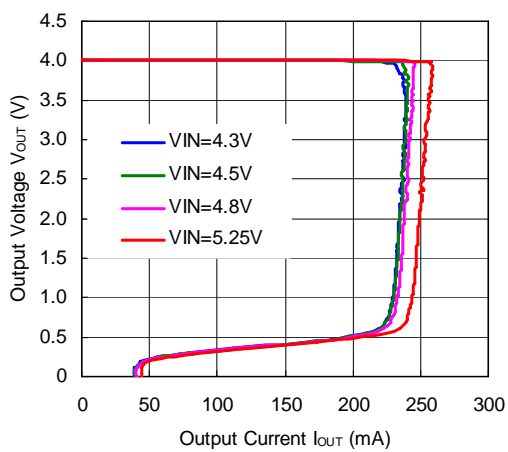
RP112x12xx



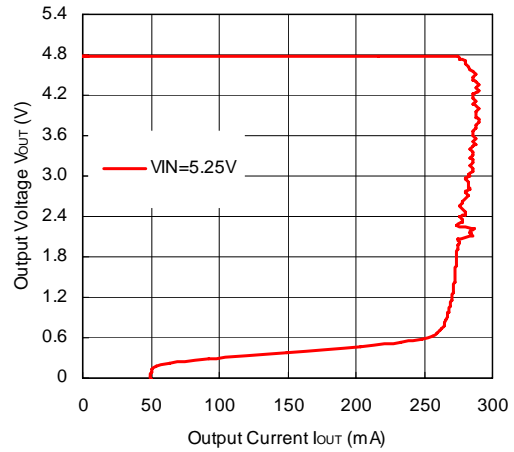
RP112x28xx



RP112x40xx

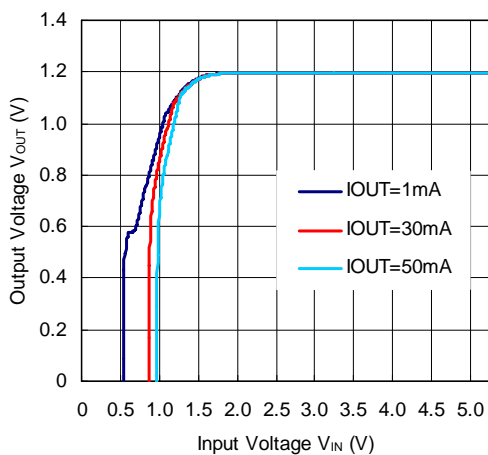


RP112x48xx

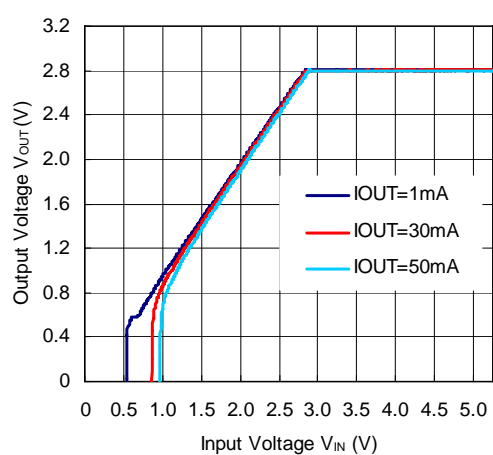


### 2) Output Voltage vs. Input Voltage (C1=Ceramic 1.0 $\mu$ F, C2=Ceramic 1.0 $\mu$ F, T<sub>opt</sub>=25°C)

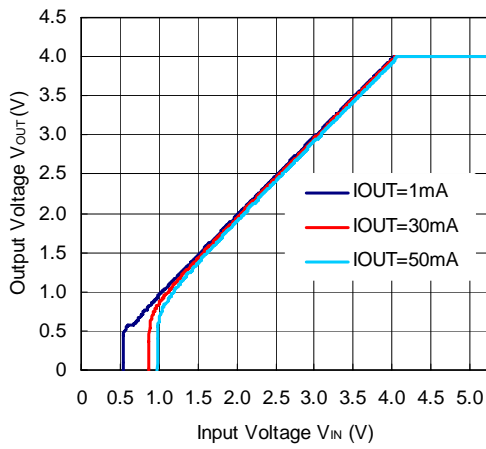
RP112x12xx



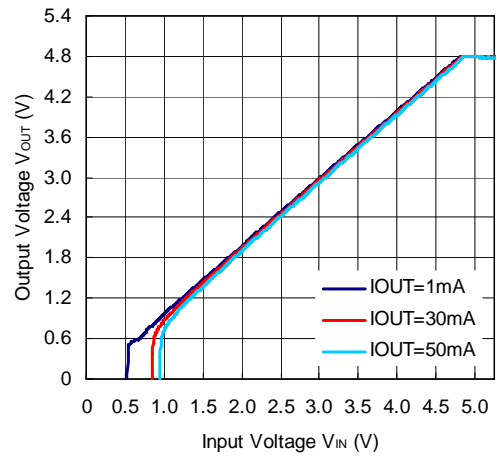
RP112x28xx



RP112x40xx

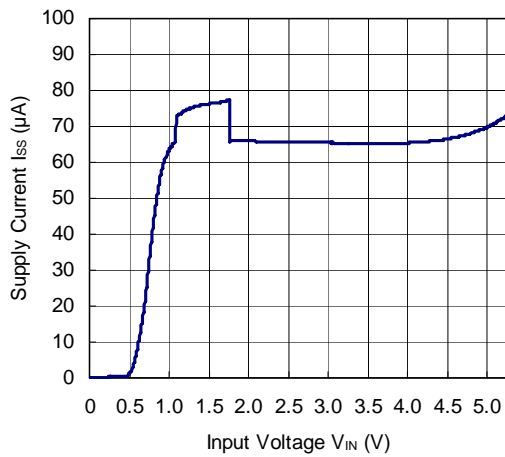


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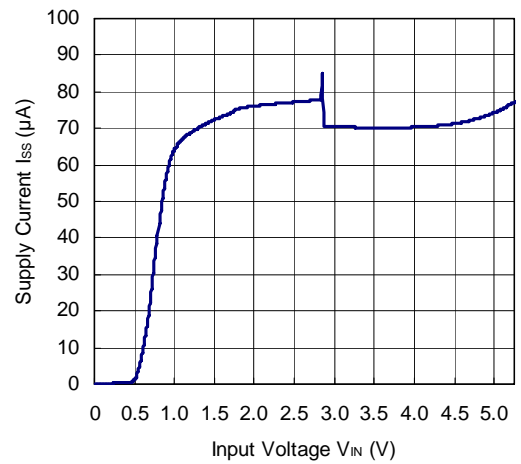


3) Supply Current vs. Input Voltage (C1=Ceramic 1.0μF, C2=Ceramic 1.0μF, T<sub>opt</sub>=25°C)

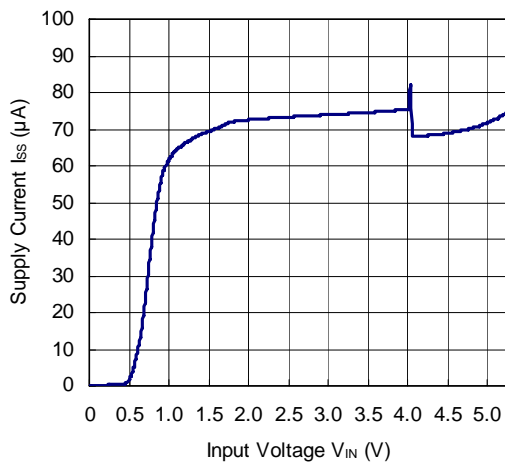
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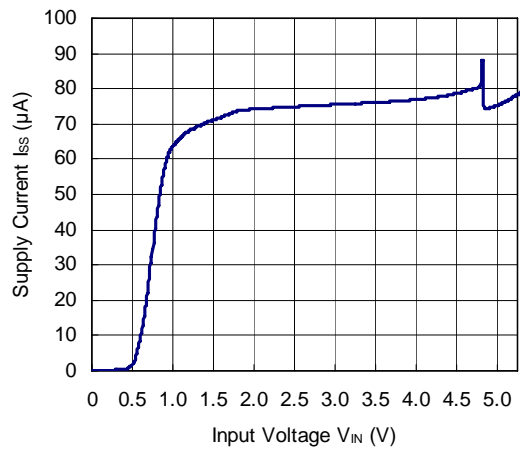
RP112x28xx



RP112x40xx



RP112x48xx

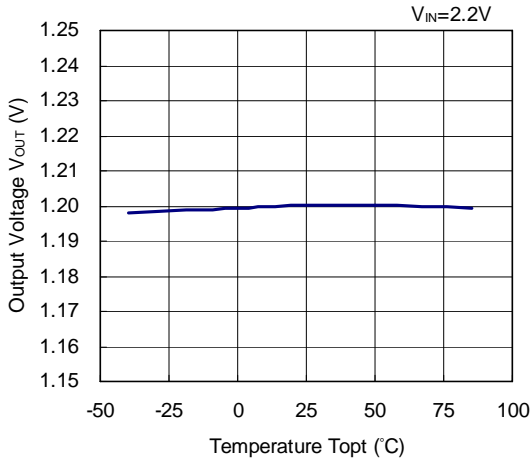


# RP112x

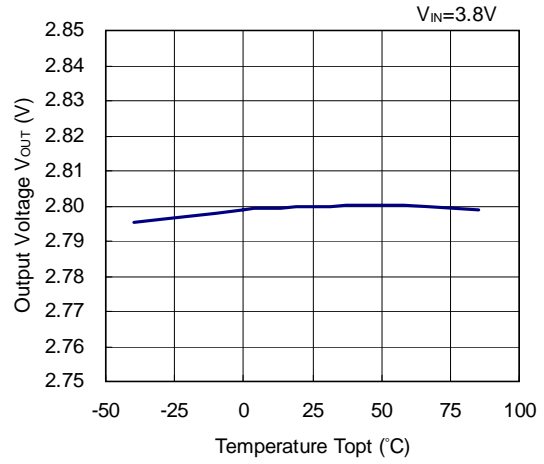
NO.EA-258-131024

## 4) Output Voltage vs. Temperature (C1=Ceramic 1.0μF, C2=Ceramic 1.0μF, I<sub>OUT</sub>=1mA)

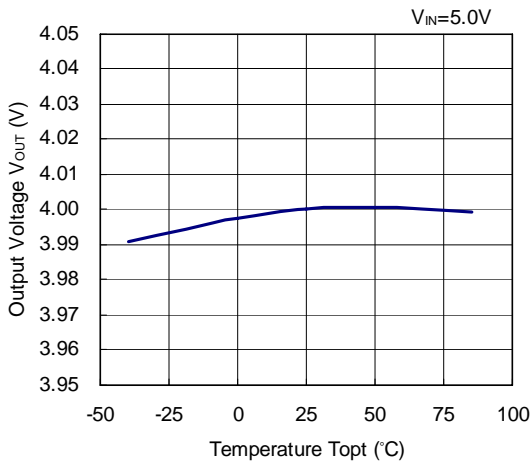
RP112x12xx



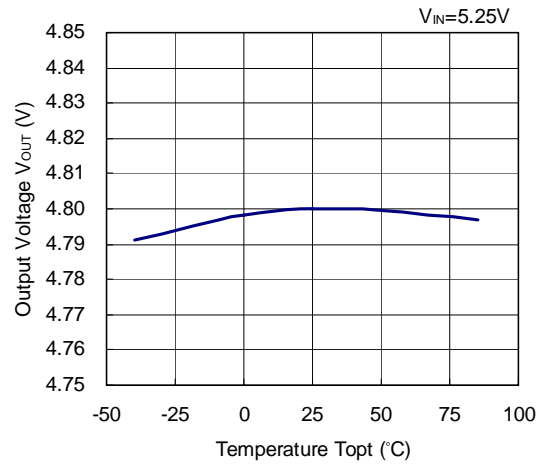
RP112x28xx



RP112x40xx

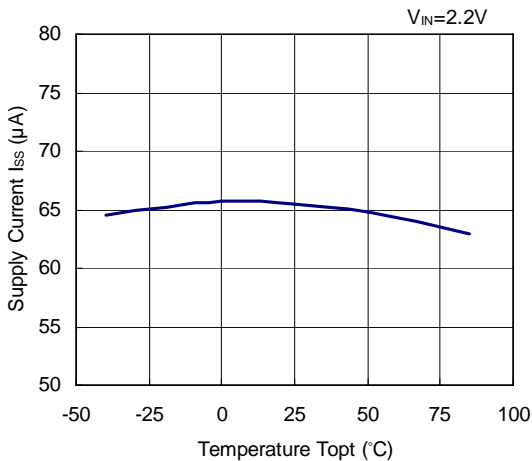


RP112x48xx

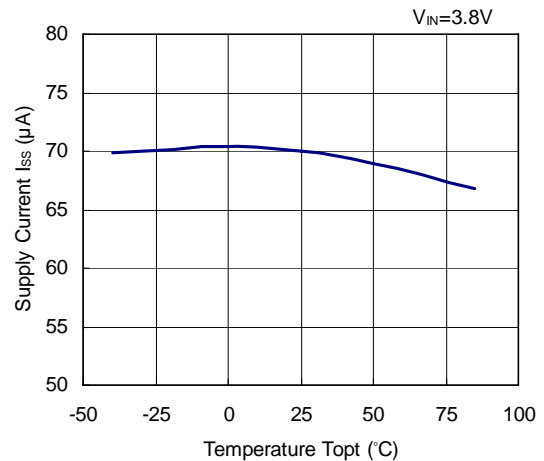


## 5) Supply Current vs. Temperature (C1=Ceramic 1.0μF, C2=Ceramic 1.0μF, I<sub>OUT</sub>=0mA)

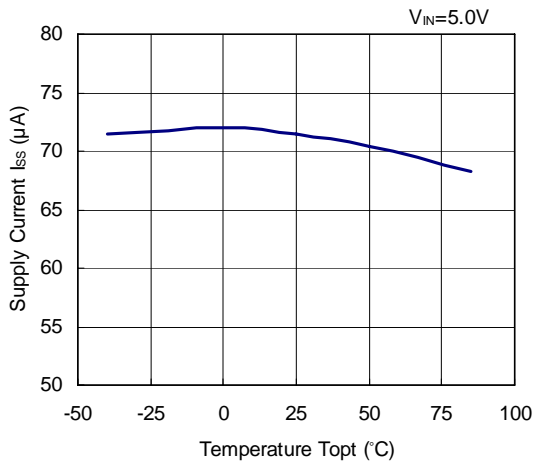
RP112x12xx



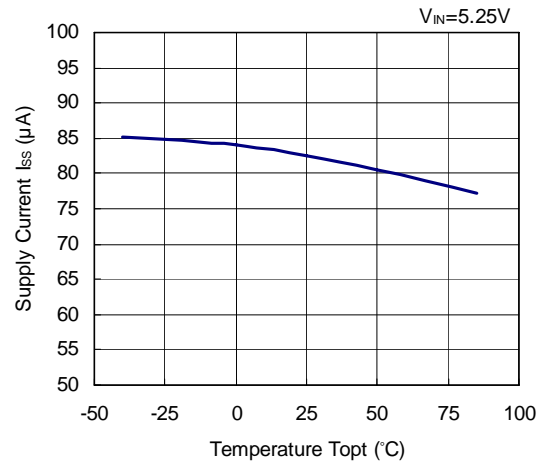
RP112x28xx



RP112x40xx

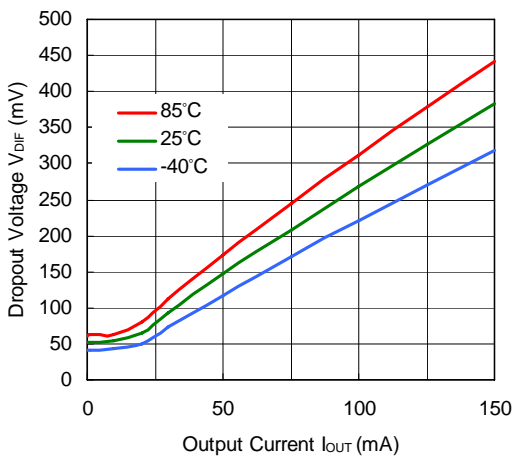


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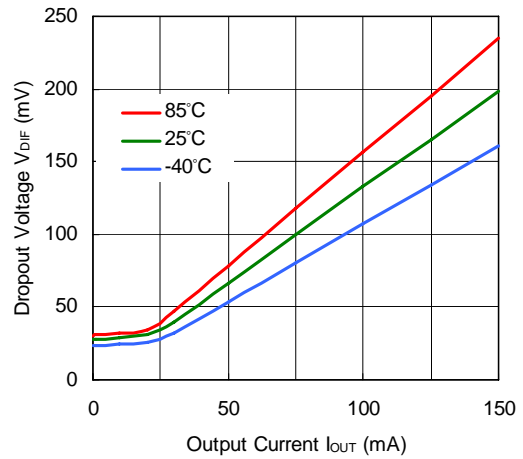


6) Dropout Voltage vs. Output Current (C1=Ceramic 1.0µF, C2=Ceramic 1.0µF)

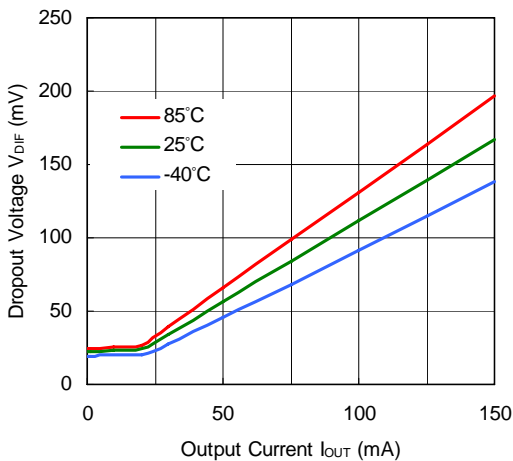
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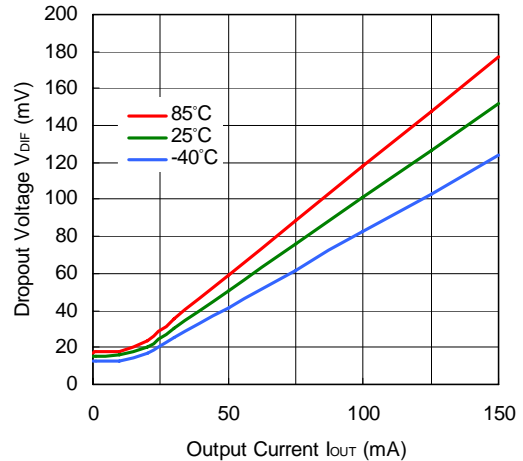
RP112x28xx



RP112x40xx



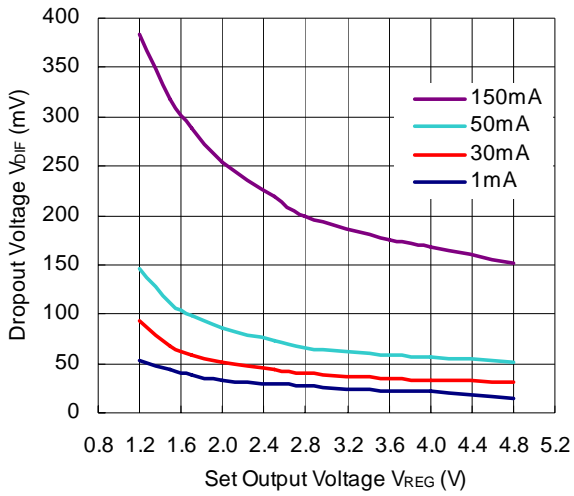
RP112x48xx



# RP112x

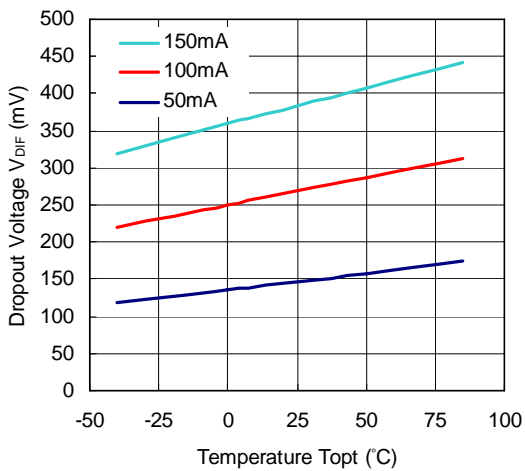
NO.EA-258-131024

## 7) Dropout Voltage vs. Set Output Voltage (C1=Ceramic 1.0μF, C2=Ceramic 1.0μF, T<sub>opt</sub>=25°C)

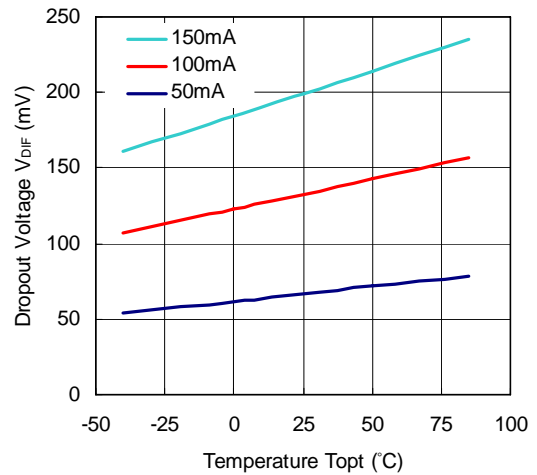


## 8) Dropout Voltage vs. Temperature (C1=Ceramic 1.0μF, C2=Ceramic 1.0μF)

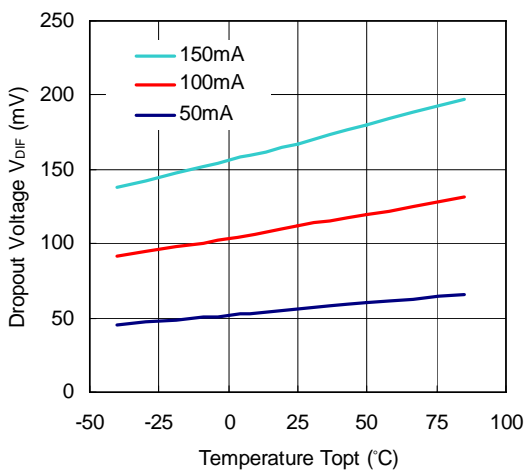
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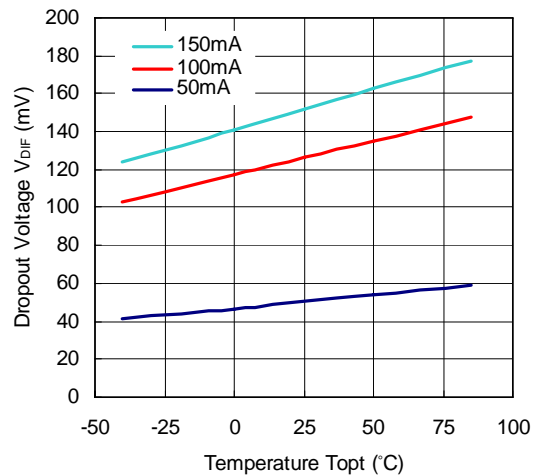
RP112x28xx



RP112x40xx

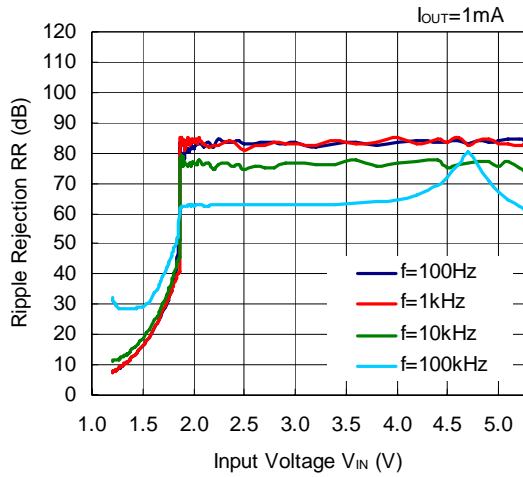


RP112x48xx

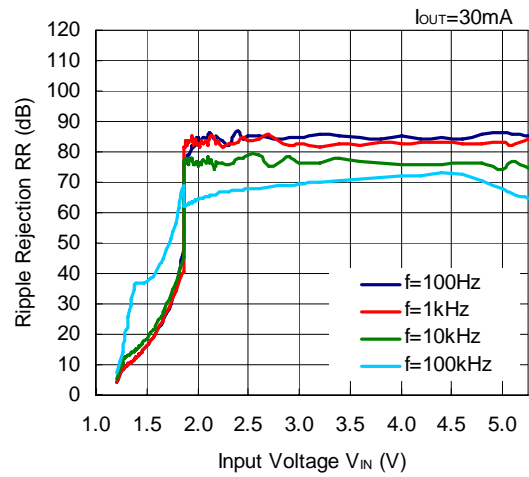


9) Ripple Rejection vs. Input Voltage (C1=none, C2=Ceramic 1.0μF, Ripple=0.2Vp-p, T<sub>opt</sub>=25°C)

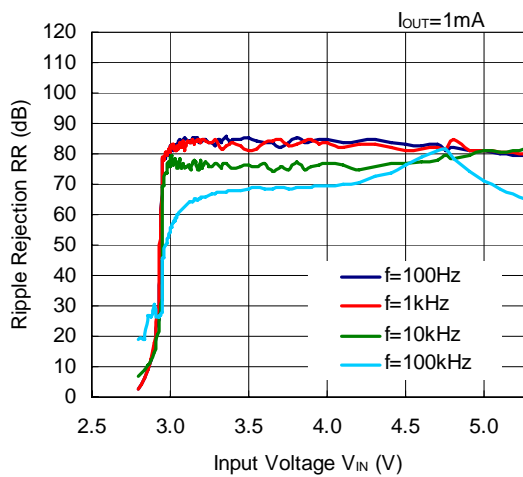
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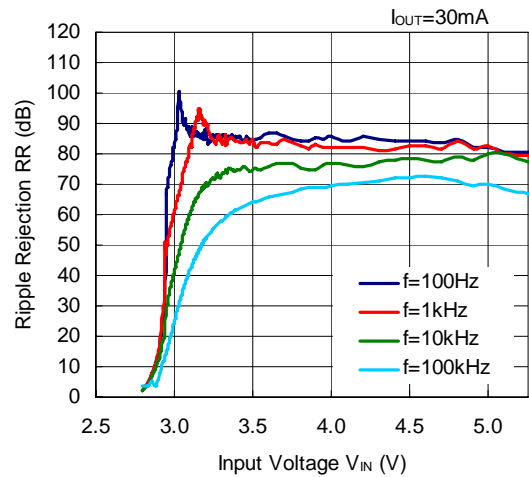
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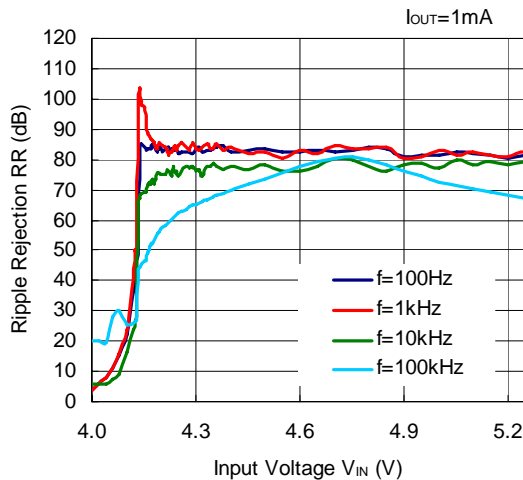
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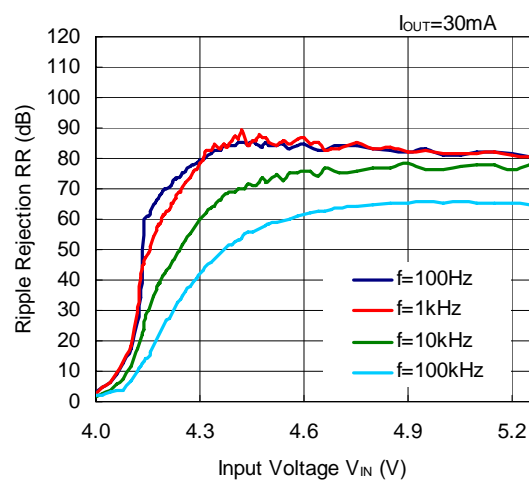
RP112x28xx



RP112x40xx



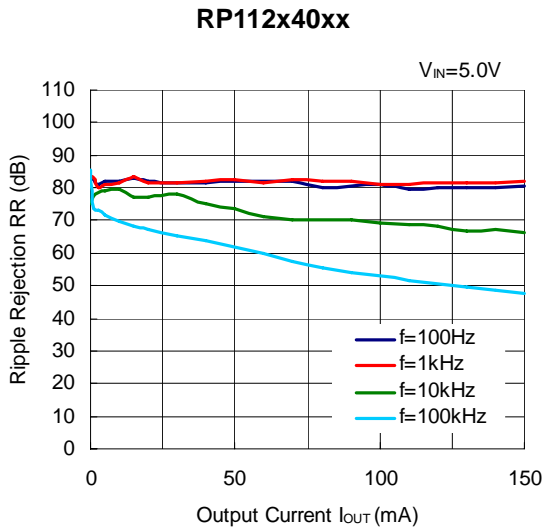
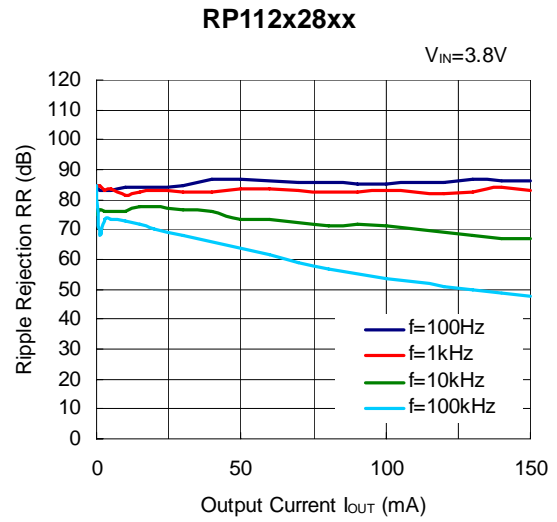
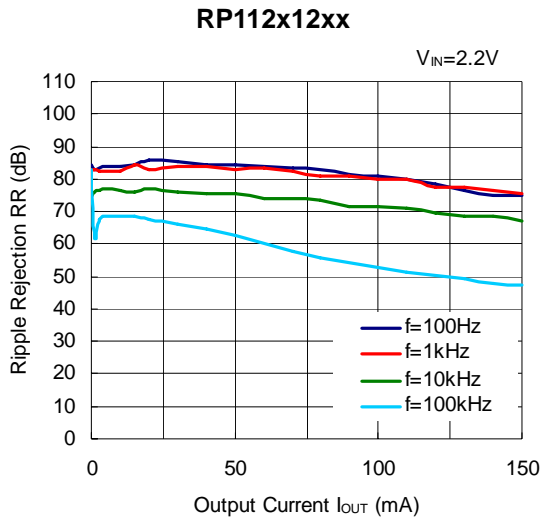
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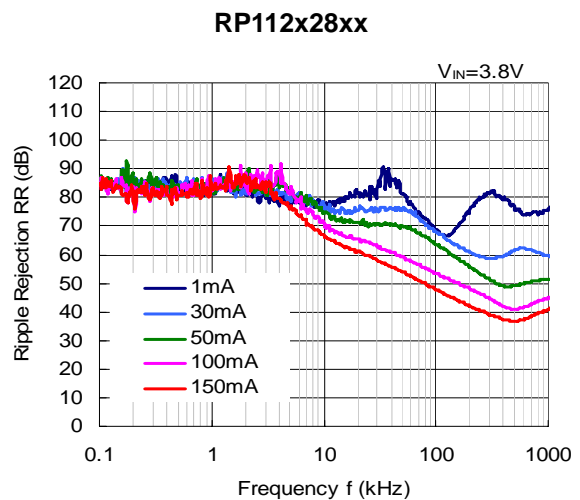
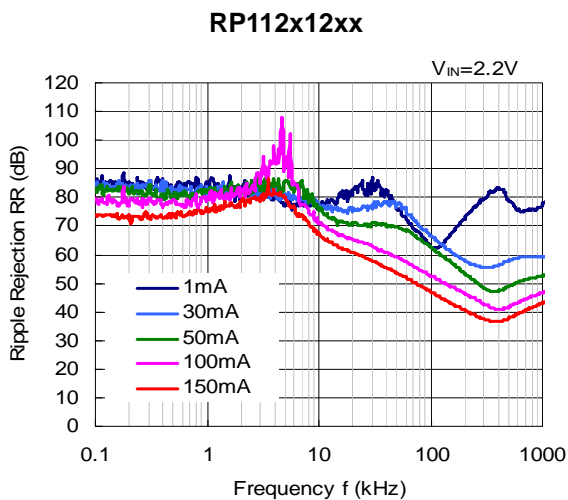
# RP112x

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## 10) Ripple Rejection vs. Output Current (C1=none, C2=Ceramic 1.0 $\mu$ F, Ripple=0.2Vp-p, T<sub>opt</sub>=25°C)

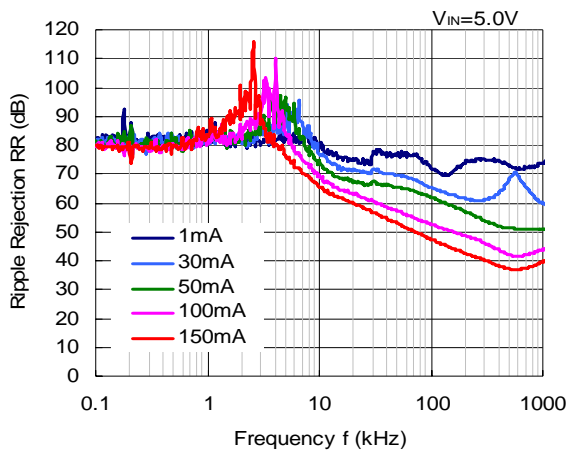


## 11) Ripple Rejection vs. Frequency (C1=none, C2=Ceramic 1.0 $\mu$ F, Ripple=0.2Vp-p, T<sub>opt</sub>=25°C)



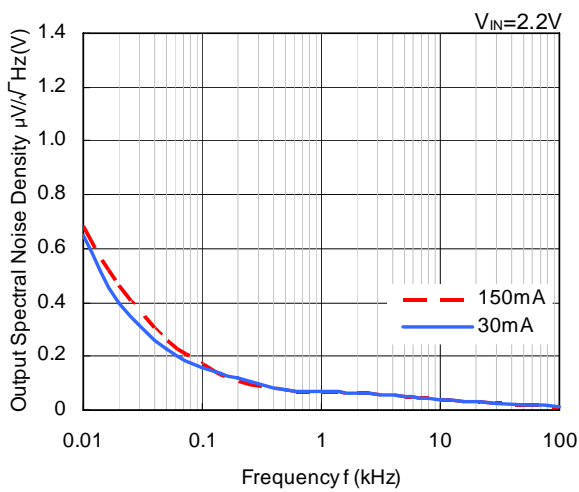


RP112x40xx

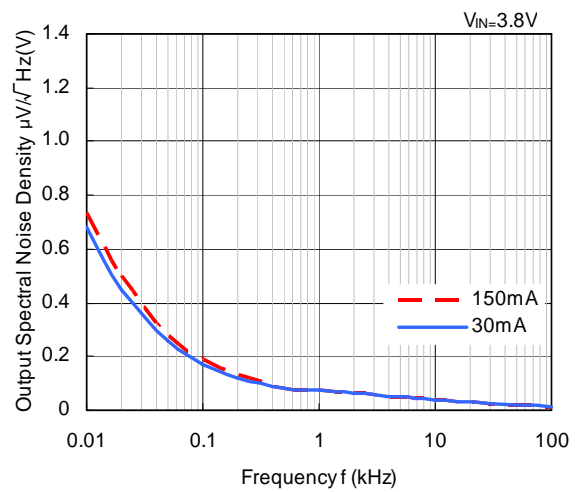


12) Output Spectral Noise Density vs. Frequency ( $C1=none, C2=Ceramic\ 1.0\mu F, T_{opt}=25^{\circ}C$ )

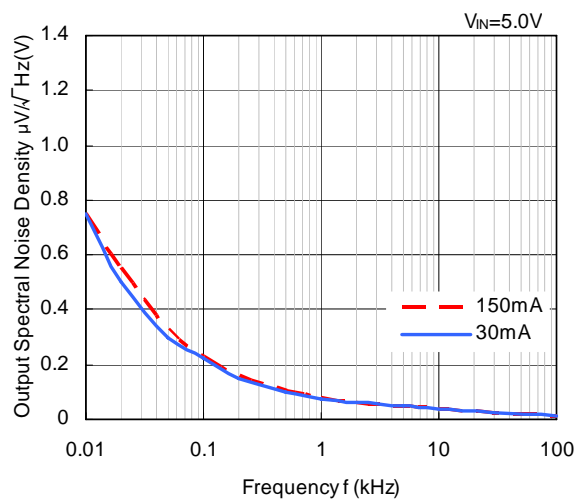
RP112x12xx



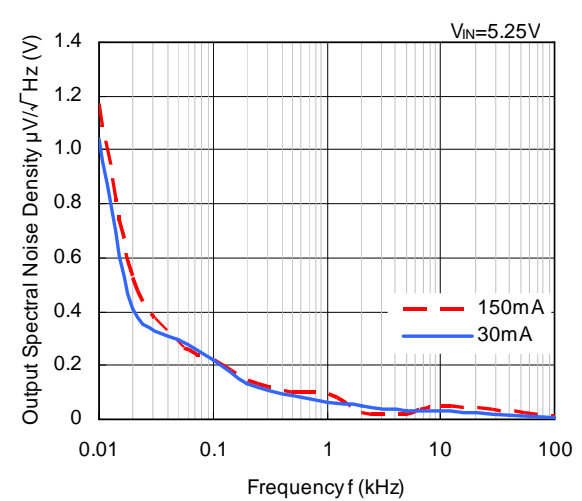
RP112x28xx



RP112x40xx



RP112x48xx

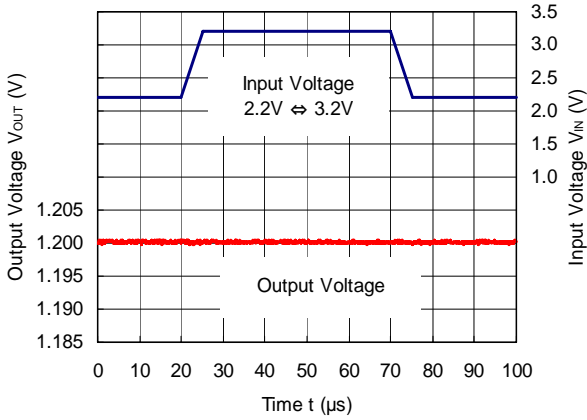


# RP112x

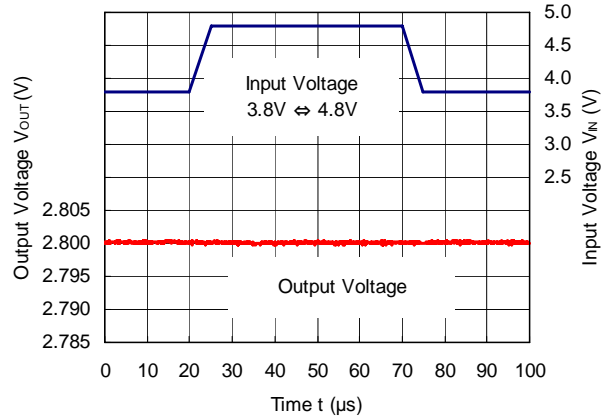
NO.EA-258-131024

## 13) Input Transient Response ( $C1$ =none, $C2$ =Ceramic $1.0\mu\text{F}$ , $I_{\text{OUT}}=30\text{mA}$ , $t_r=t_f=5.0\mu\text{s}$ , $T_{\text{opt}}=25^\circ\text{C}$ )

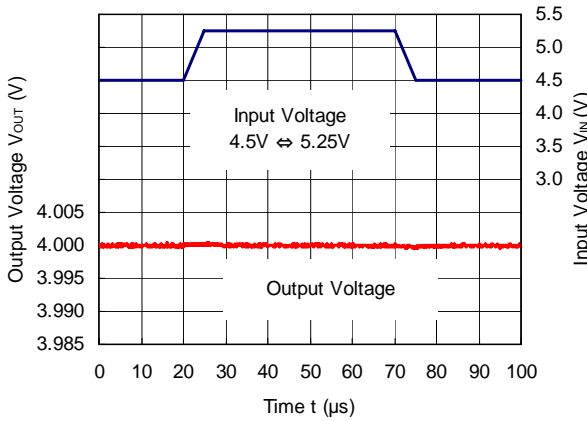
### RP112x12xx



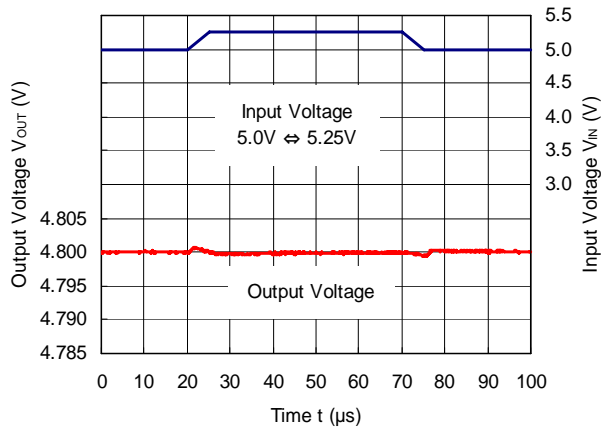
### RP112x28xx



### RP112x40xx

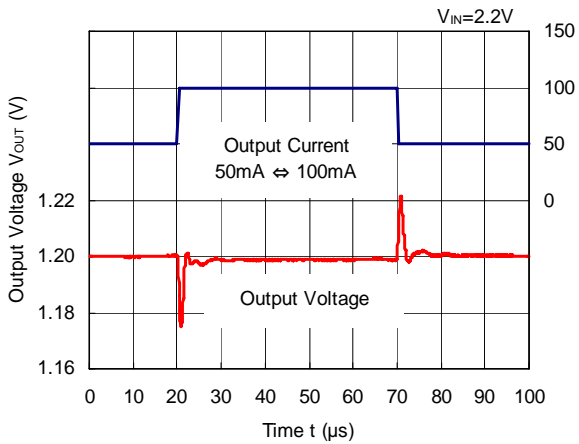


### RP112x48xx

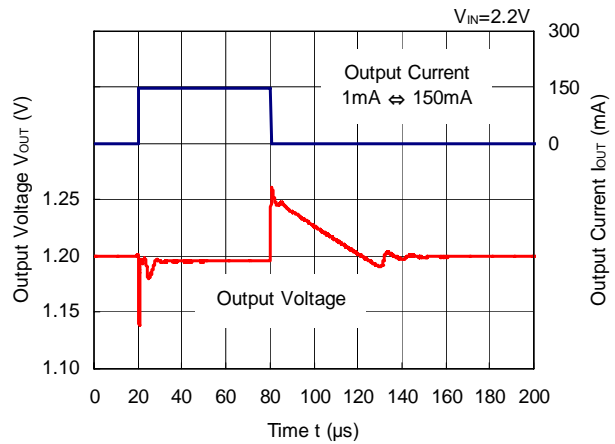


## 14) Load Transient Response ( $C1$ =Ceramic $1.0\mu\text{F}$ , $C2$ =Ceramic $1.0\mu\text{F}$ , $t_r=t_f=0.5\mu\text{s}$ , $T_{\text{opt}}=25^\circ\text{C}$ )

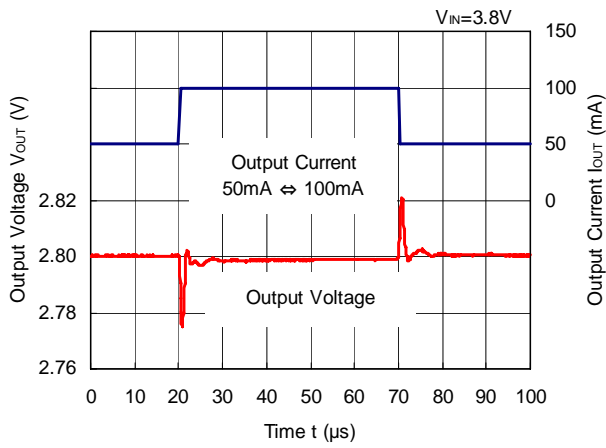
### RP112x12xx



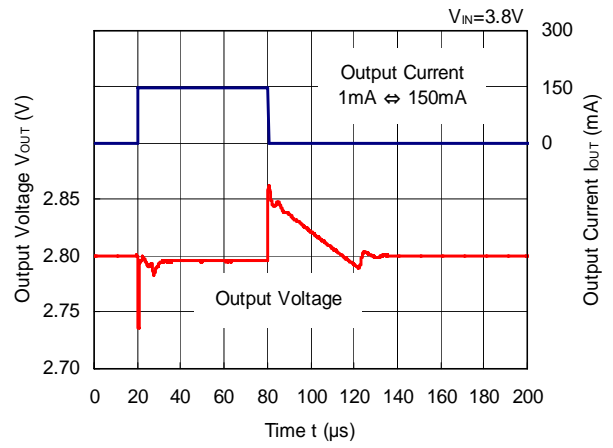
### RP112x12xx



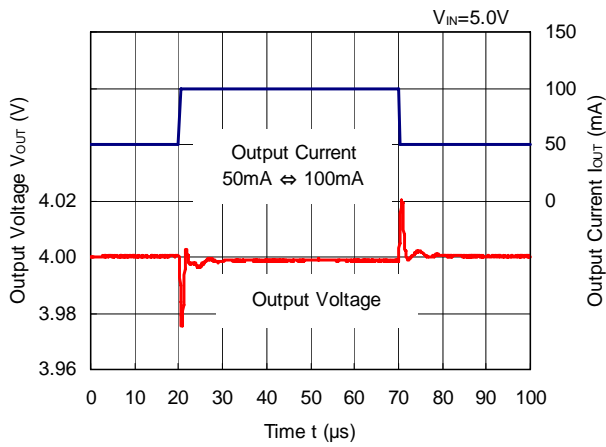
RP112x28xx



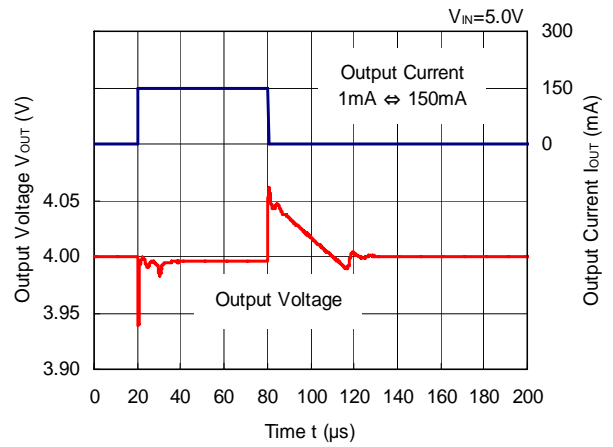
RP112x28xx



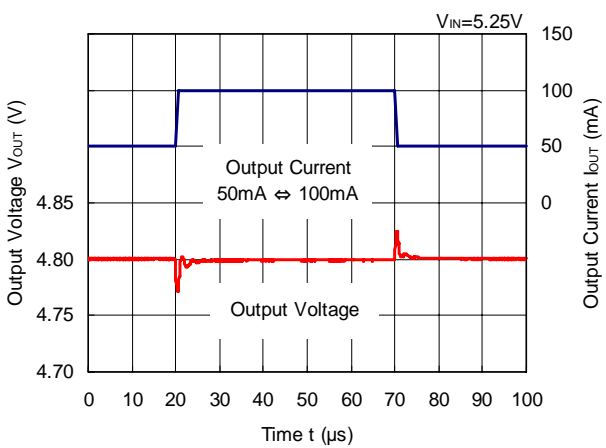
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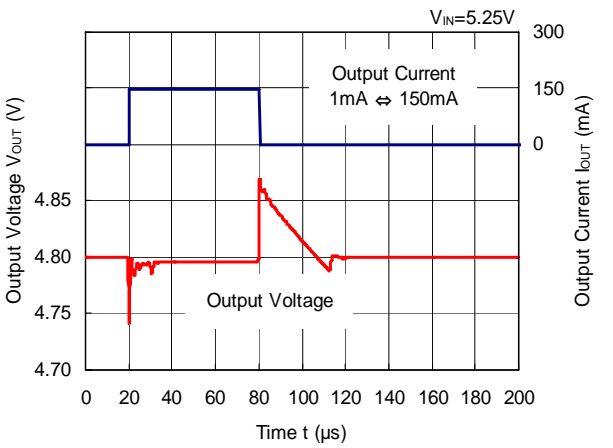
RP112x40xx



RP112x48xx



RP112x48xx

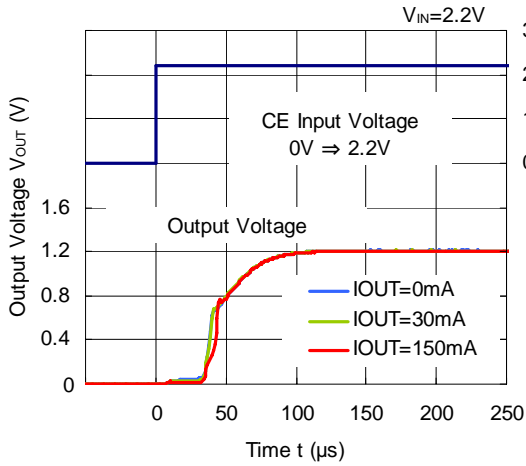


# RP112x

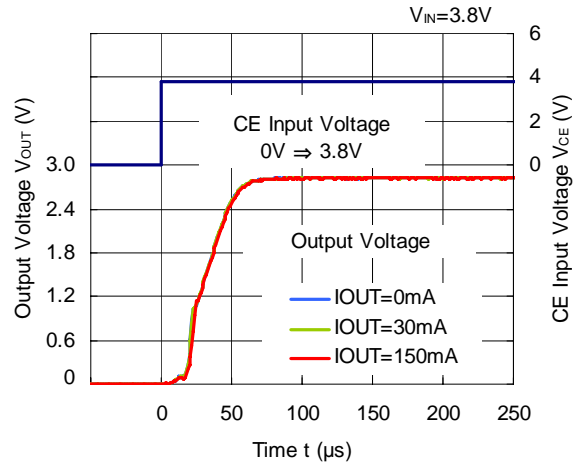
NO.EA-258-131024

## 15) Turn on Speed with CE pin (C1=Ceramic 1.0 $\mu$ F, C2=Ceramic 1.0 $\mu$ F, T<sub>opt</sub>=25°C)

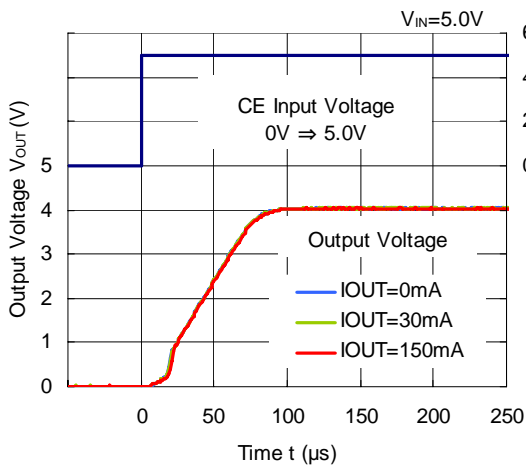
### RP112x12xx



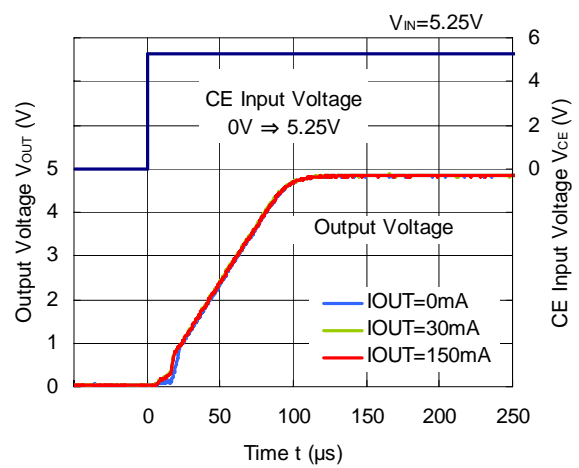
### RP112x28xx



### RP112x40xx

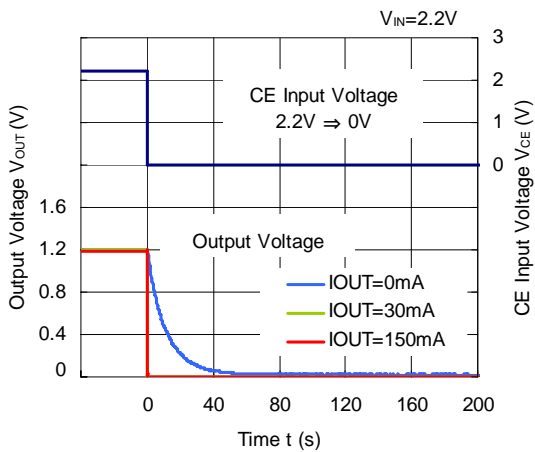


### RP112x48xx

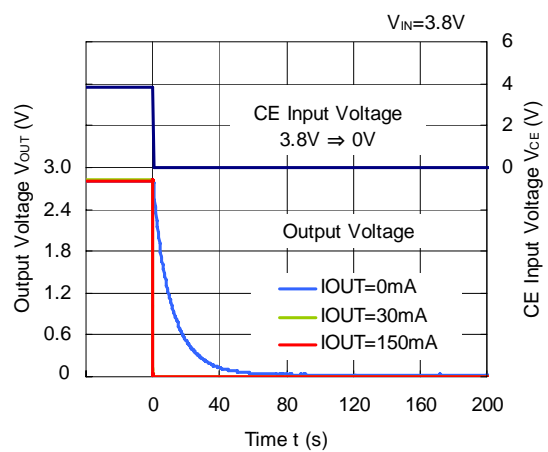


## 16) Turn off Speed with CE pin (B Version) (C1=Ceramic 1.0 $\mu$ F, C2=Ceramic 1.0 $\mu$ F, T<sub>opt</sub>=25°C)

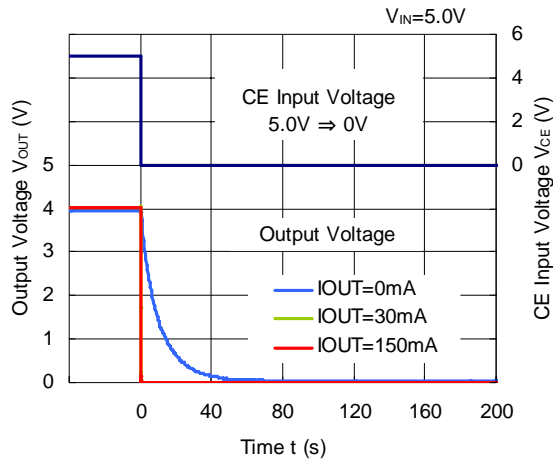
### RP112x12xx



### RP112x28xx

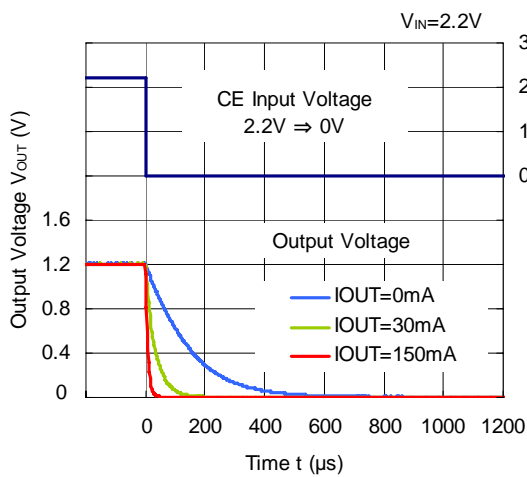


RP112x40xB

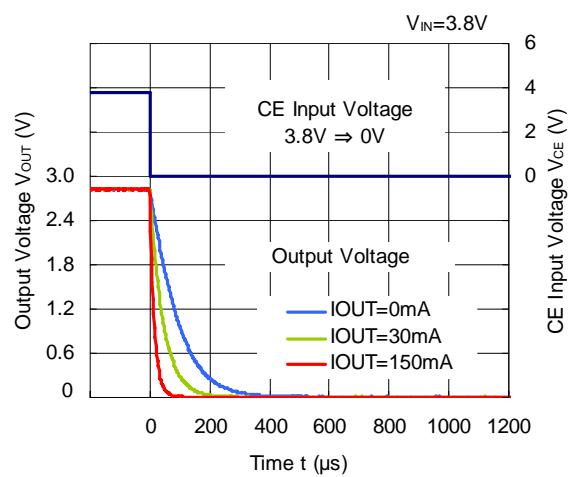


17) Turn off Speed with CE pin (D Version) (C1=Ceramic 1.0 $\mu$ F, C2=Ceramic 1.0 $\mu$ F,  $T_{opt}=25^{\circ}C$ )

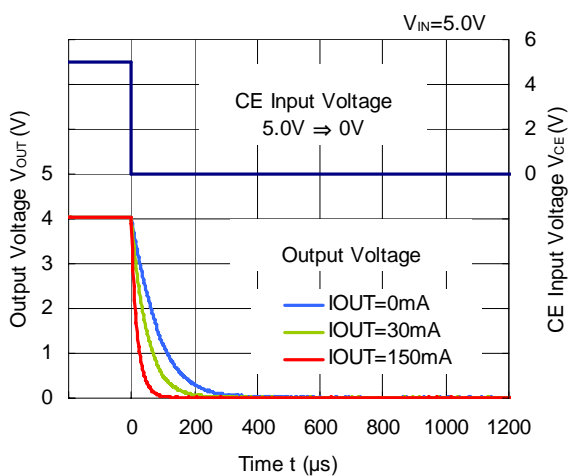
RP112x12xD



RP112x28xD

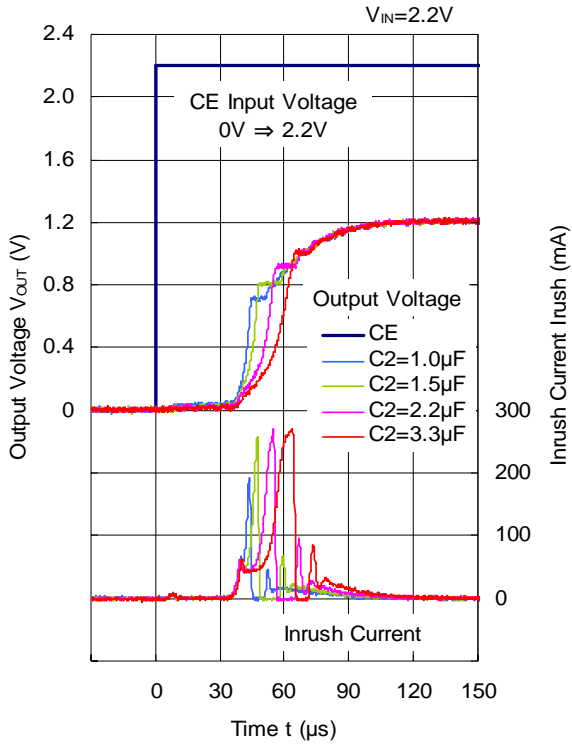


RP112x40xD

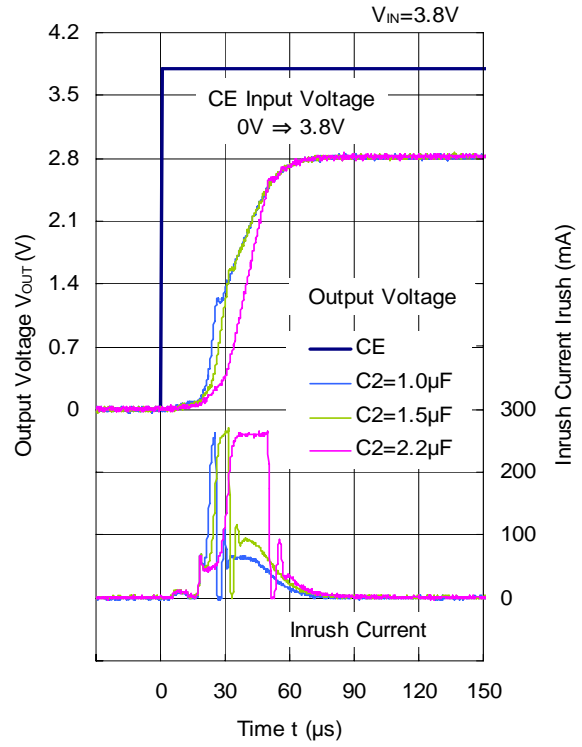


18) Inrush Current (C1=Ceramic 1.0μF, I<sub>OUT</sub>=0mA, T<sub>opt</sub>=25°C)

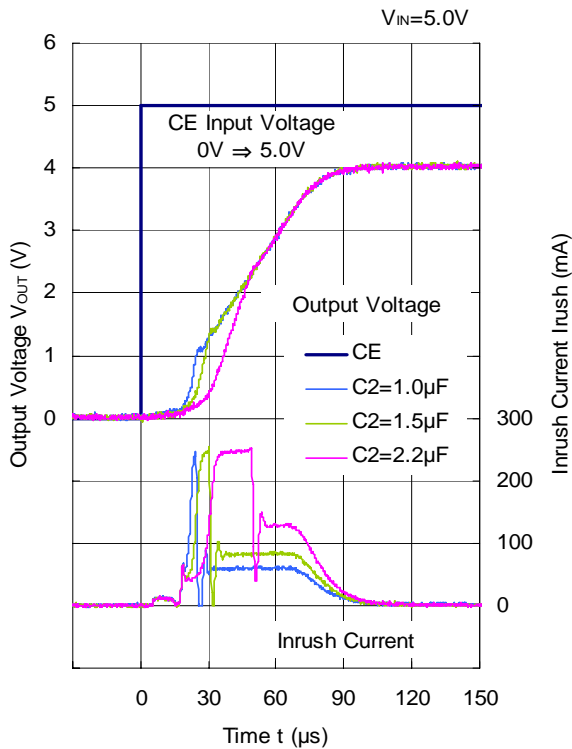
RP112x12xx



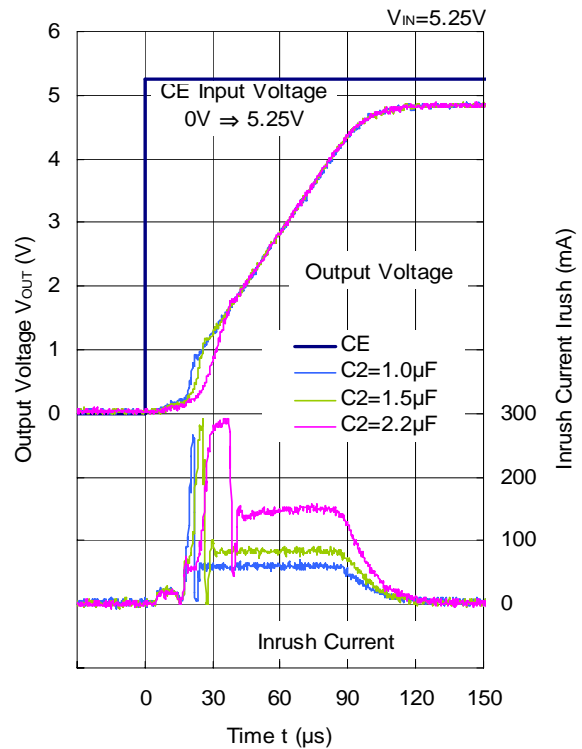
RP112x28xx



RP112x40xx



RP112x48xx



## ESR vs. Output Current

When using these ICs, consider the following points:

The relations between  $I_{OUT}$  (Output Current) and ESR of an output capacitor are shown below.

The conditions when the white noise level is under  $40\mu\text{V}$  (Avg.) are marked as the hatched area in the graph.

### Measurement Conditions

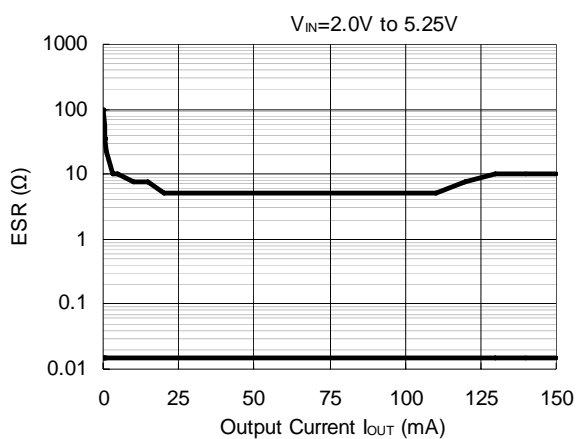
Frequency Band : 10Hz to 2MHz

Temperature :  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$

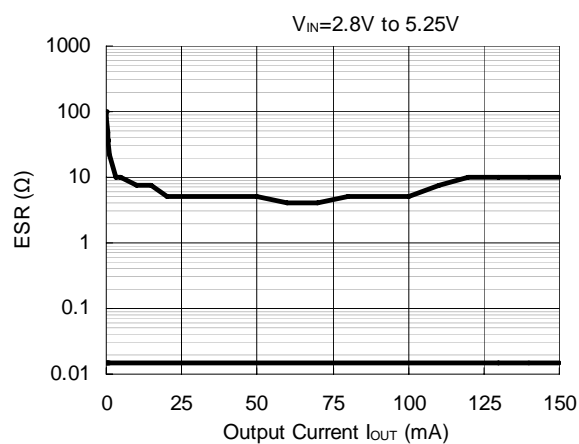
Hatched Area : Noise level is under  $40\mu\text{V}$ (Avg.)

C1,C2 :  $1.0\mu\text{F}$  or more

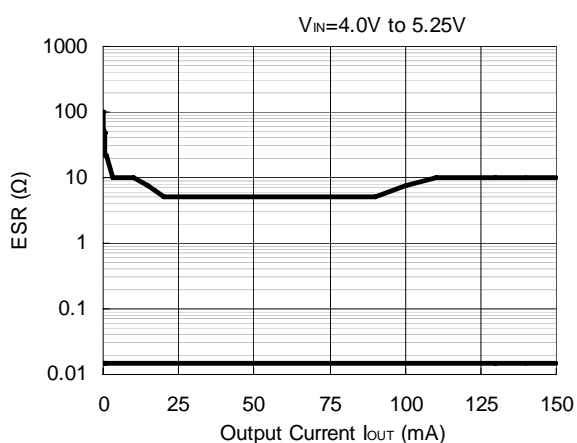
**RP112x12xx**



**RP112x28xx**



**RP112x40xx**





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