USB HIGH-SIDE POWER SWITCH

NO.EA-188-161207

OUTLINE

The R5524x is a CMOS-based high-side MOSFET switch IC which conforms to the universal serial bus (USB) standard. The device is suitable for protecting a USB power source.

By using an Nch MOSFET with low On-resistance (Typ. 100 mΩ) as a switching transistor, the device can provide low dropout voltage.

Internally, the device consists of an overcurrent limiting circuit, a thermal shutdown circuit, an undervoltage lockout (UVLO) circuit and a reverse current protection circuit. The device also consists of an internal delay circuit to prevent the output of false flag signals caused by inrush current.

To achieve simplification of layout design, the overcurrent detection accuracy has been improved.

The R5524x is offered in a 5-pin SOT-23-5 package and a 6-pin DFN(PLP)1820-6 package which achieve the smallest possible footprint solution on boards where area is limited.

FEATURES

- N-channel MOS High-Side Switch IC
- Switch ON Resistance ····· Typ. 100 mΩ at 5 V Input
- Current Limit Threshold ····· Min. 650 mA[*1], Min. 1.25 A[*2]
- Overcurrent Limit ····· Min. 550 mA
- Flag Delay Time ····· Typ. 20 ms
- Under-voltage Lockout (UVLO) Circuit
- Thermal Shutdown Circuit
- Reverse Current Protection Circuit
- Package ····· SOT-23-5, DFN(PLP)1820-6[*3]

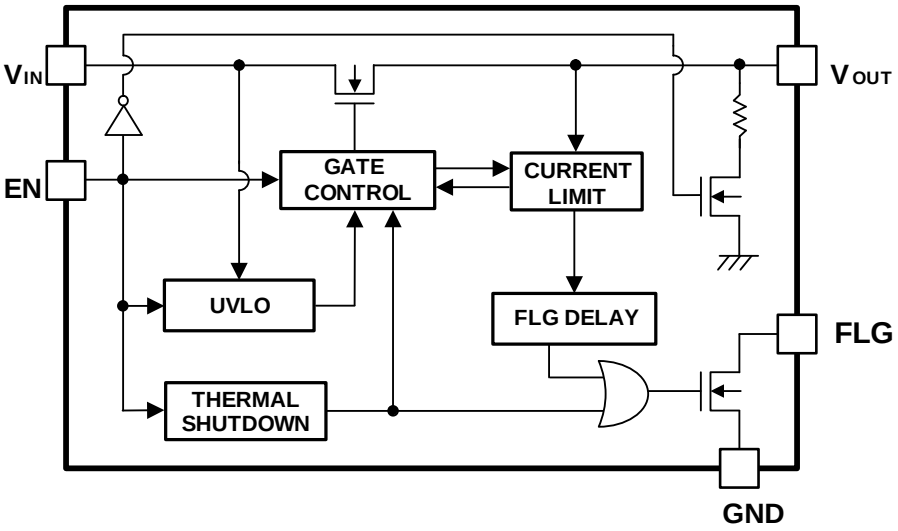
APPLICATIONS

- PCs and PC Peripherals
- Digital Televisions (DTV)
- Set Top Boxes (STB)
- Printers
- PDA
- Game Consoles

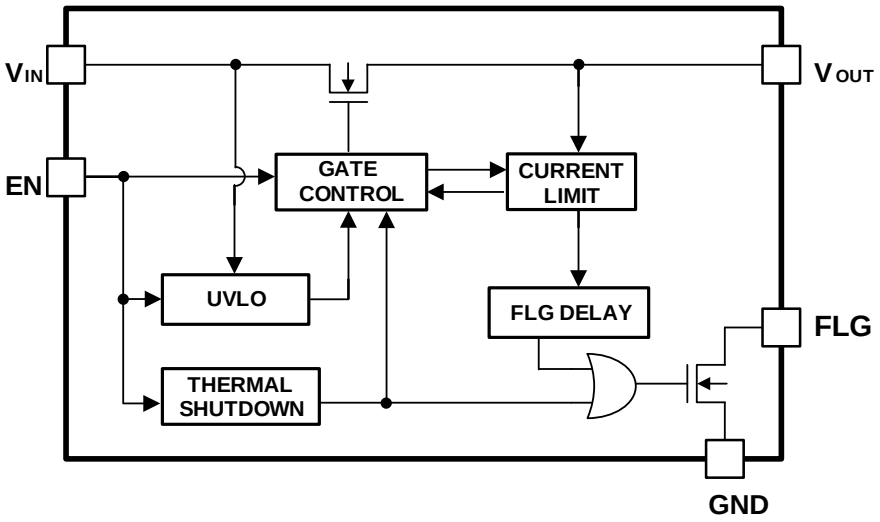
[*1] only for R5524x001A/B, R5524x002A/B
[*2] only for R5524N004A
[*3] only for R5524K001x, R5524K002x

BLOCK DIAGRAMS

R5524xxxxA Block Diagram



R5524xxxxB Block Diagram



SELECTION GUIDE

The overcurrent limit protection type, the current limit threshold and the auto discharge options[*1] for the ICs are user-selectable options.

Selection Guide

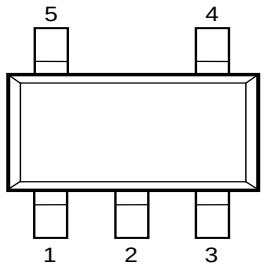
Product Name	Package	Quantity per Reel	Pb Free	Halogen Free
R5524N00x∗-TR-FE	SOT-23-5	3,000 pcs	Yes	Yes
R5524K00x∗-TR	DFN(PLP)1820-6	5,000 pcs	Yes	Yes

x: Specify the combination of Overcurrent Limit Protection type and Current Limit Threshold.
1: Latch-off Type, Current Limit Threshold: Min. 650 mA
2: Constant Current Type, Current Limit Threshold: Min. 650 mA
4: Cosntant Current Type, Current Limit Threshold: Min. 1.25 A[*2]

∗: Specify auto-discharge options.
A: Auto-discharge included
B: Auto-discharge not included

[*1] Auto-discharge function quickly lowers the output voltage to 0 V, when the chip enable signal is switched from the active mode to the standby mode, by releasing the electrical charge accumulated in the external capacitor.
[*2] only for R5524N004A

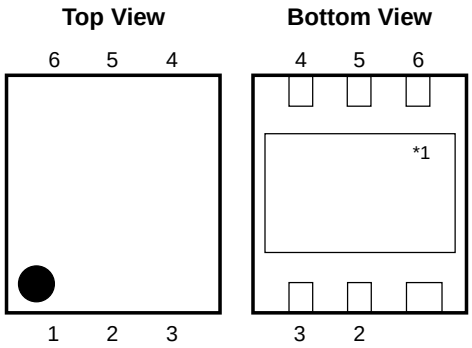
PIN DESCRIPTIONS



SOT-23-5 Pin Configuration

SOT23-5 Pin Description

Pin No.	Symbol	Description
1	V_{IN}	Input Pin
2	GND	Ground Pin
3	EN	Chip Enable Pin, Active-high
4	FLG	Flag Pin, Open Drain Output
5	V_{OUT}	Output Pin



DFN(PLP)1820-6 Pin Configuration

DFN(PLP)1820-6 Pin Description

Pin No.	Symbol	Description
1	V_{OUT}	Output Pin
2	NC	No Connection
3	FLG	Flag Pin, Open Drain Output
4	EN	Enable Pin, Active-high
5	GND	Ground Pin
6	V_{IN}	Input Pin

*1 The tab on the bottom of the package enhances thermal performance and is electrically connected to GND (substrate level). It is recommended that the tab be connected to the ground plane on the board, or otherwise be left floating.

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings

Symbol	Item		Rating	Unit
V_{IN}	Input Voltage		6.0	V
V_{EN}	Enable Pin Input Voltage		−0.3 to 6.0	V
V_{FLG}	Flag Pin Voltage		−0.3 to 6.0	V
I_{FLG}	Flag Pin Current		14	mA
V_{OUT}	Output Pin Voltage		−0.3 to 6.0	V
I_{OUT}	Output Current		Internally Controlled	
P_D	Power Dissipation (Standard Land Pattern)*1	SOT-23-5	420	mW
		DFN(PLP)1820-6	880	mW
Ta	Operating Temperature Range		−40 to 85	°C
Tstg	Storage Temperature Range		−55 to 125	°C

*1 Refer to *PACKAGE INFORMATION* for detailed information.

ABSOLUTE MAXIMUM RATINGS

Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause the permanent damages and may degrade the life time and safety for both device and system using the device in the field. The functional operation at or over these absolute maximum ratings is not assured.

ELECTRICAL CHARACTERISTICS

The specifications surrounded by ☐ are guaranteed by design engineering at −40°C ≤ Ta ≤ 85°C.

Electrical Characteristics (Ta = 25°C)

Symbol	Item	Conditions		Min.	Typ.	Max.	Unit
V_{IN}	Input Voltage			2.7		5.5	V
I_{DD1}	Supply Current (Active Mode)	V_{OUT} = OPEN, EN = "H", V_{IN} = 5 V			110	180	µA
I_{DD2}	Supply Current (Standby Mode)	V_{OUT} = OPEN, EN = "L", V_{IN} = 5 V			0.1	1.0	µA
R_{ON}	Switch On Resistance	V_{IN} = 5 V, I_{OUT} = 500 mA			100	150	mΩ
ton	Output Turn-on Delay	V_{IN} = 5 V, R_L = 60 Ω			400		µs
toff	Output Turn-off Delay	V_{IN} = 5V, R_L = 60 Ω			50		µs
V_{UVLO}	UVLO Release Voltage	V_{IN} Rising		2.3	2.5	2.7	V
V_{HYS}	UVLO Hysteresis Range	V_{IN} Falling			0.1		V
I_{TH}	Current Limit Threshold	R5524x001A/ 001B R5524x002A/ 002B	V_{IN} = 5 V	650	800	980	mA
		R5524N004A	V_{IN} = 5 V	1.25	1.55	1.85	A
			V_{IN} = 5 V, Ta = 0 to 70°C	1.2	1.55	1.9	
I_{LIM}	Overcurrent Limit	V_{IN} = 5 V, V_{OUT} = 0 V, after 5 ms		550	650	800	mA
t_{FD}	Flag Delay Time*1	V_{IN} = 5 V, starts when overcurrent is detected and ends when FLG = "L"		7	20	30	ms
T_{TSD}	Thermal Shutdown Temperature	Junction Temperature			135		°C
T_{TSR}	Thermal Shutdown Released Temperature	Junction Temperature			120		°C
I_{EN}	Enable Pin Input Current				0.01	1.0	µA
V_{EN1}	Enable Pin Input Voltage 1	V_{EN} Rising		2.0		6.0	V
V_{EN2}	Enable Pin Input Voltage 2	V_{EN} Falling		−0.3		0.8	V
I_{LO}	Output Leakage Current				0.1	1.0	µA
V_{LF}	Flag "L" Output Voltage	I_{SINK} = 1 mA				0.4	V
I_{FOF}	Flag Off Current	V_{FLG} = 5.5 V			0.01	1.0	µA
I_{REV}	Reverse Leakage Current	V_{IN} = 0 V, V_{OUT} = 5.5 V				50	µA
R_{LOW}	Nch. On-resistance for Auto Discharge (R5524x00xA)				450		Ω

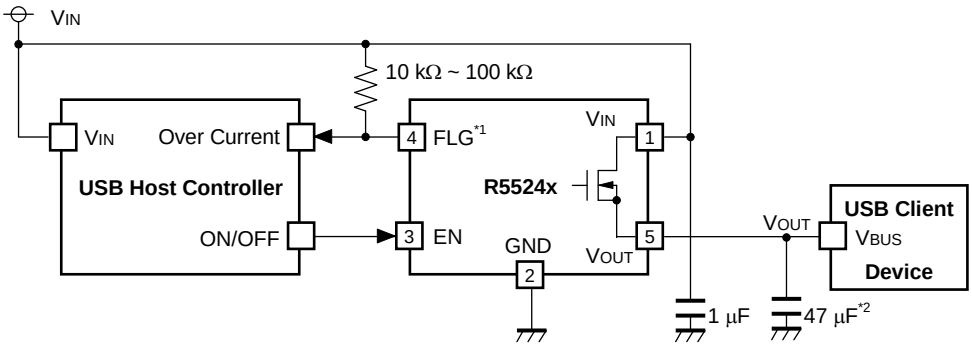
All test items listed under Electrical Characteristics are done under the pulse load condition (Tj ≈ Ta = 25°C) except Thermal Shutdown Temperature and Thermal Shutdown Released Temperature.

*1 Flag Delay Time is dependent on Input Voltage.

RECOMMENDED OPERATING CONDITIONS (ELECTRICAL CHARACTERISTICS)

All of electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating conditions. The semiconductor devices cannot operate normally over the recommended operating conditions, even if when they are used over such conditions by momentary electronic noise or surge. And the semiconductor devices may receive serious damage when they continue to operate over the recommended operating conditions.

TYPICAL APPLICATION



R5524x Typical Application

*1 FLG pin is Nch. Open Drain Output.

*2 A 47 µF or more output capacitor is recommended. According to a USB standard, a 120 µF or more output capacitor is required.

TECHNICAL NOTES

Bypass Capacitor

A 0.1µF to 1 µF bypass capacitor between the V_{IN} pin and the GND pin, close to the device, is recommended. This precaution reduces power supply transients that may cause ringing on the input.

Pull-up Resistor of FLG Pin

A 10 kΩ to 100 kΩ pull-up resistor is recommended for the FLG pin.

R5524x001A/001B

The R5524x001A/001B is equipped with a latch-off function which requires initialization before start-up.

Case 1: Start-up by EN Pin Control

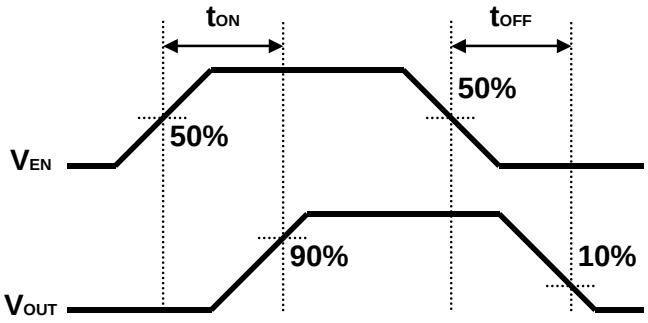
EN pin must be enabled with the delay of 10 µs or more against 90% of V_{IN} voltage rising edge.

Case 2: Start-up by EN Pin Tied to V_{IN} Pin

Slew rate of V_{IN} must be 40 µs/V or slower.

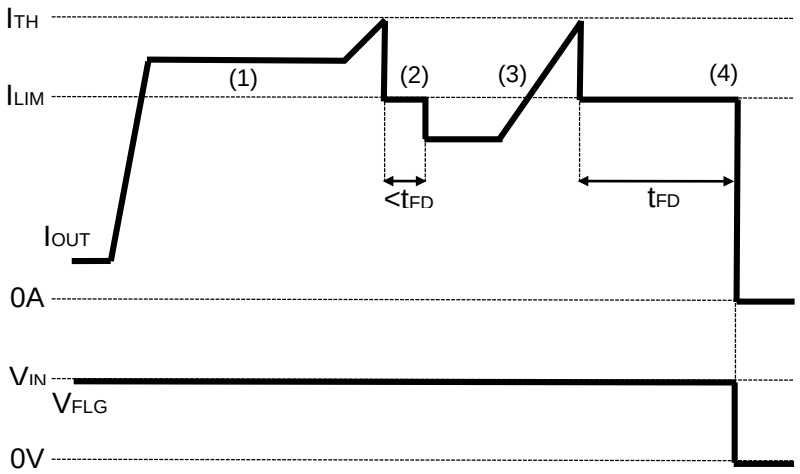
TIMING CHART

Output On-time and Output Off-time



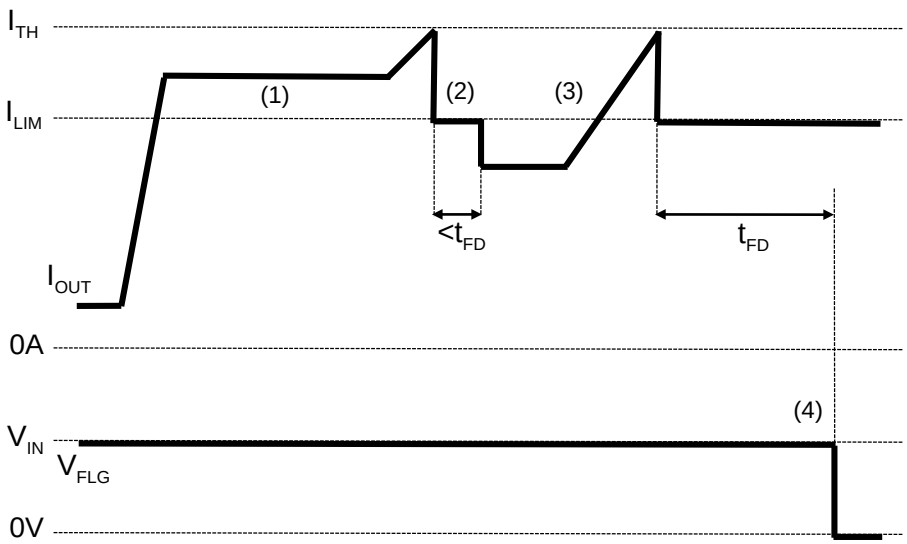
R5524x Timing Chart

Flag Delay Time



R5524x001A/001B Timing Chart (Latch-off Type)

(1) When the I_{OUT} is I_{TH} or less, the current is not limited.
(2) Once the I_{OUT} reaches to I_{TH}, the I_{OUT} is limited by I_{LIM}.
(3) When the I_{OUT} drops to I_{LIM} or less within the t_{FD} time, the current limit is released. The current is not limited until the I_{OUT} exceeds I_{TH} again.
(4) When the I_{OUT} reaches to I_{TH} and it is limited by I_{LIM} for t_{FD} or more, the switch transistor turns off and V_{FLG} becomes “Low”.



R5524x002A/002B and R5524N004A Timing Chart (Constant Current Type)

(1) When I_{OUT} is I_{TH} or less, the current is not limited.
(2) Once the I_{OUT} reaches to I_{TH}, the I_{OUT} is limited by I_{LIM}.
(3) When the I_{OUT} drops to I_{LIM} or less within the t_{FD} time, the current limit is released. The current is not limited until the I_{OUT} exceeds I_{TH} again.
(4) When the I_{OUT} reaches to I_{TH} and it is limited by I_{LIM} for t_{FD} or more, the V_{FLG} becomes “Low”.

Overcurrent Limiting Function

The R5524x001A/001B has the built-in latch-off type over-current limit circuit. When the over-current is detected, the protection circuit becomes active and the switch-transistor is turned OFF. The latch function is released if the input voltage value is exceeded in the release threshold of the UVLO circuit value after when it became lower than the detection threshold of the UVLO circuit value; or the EN pin set to the enabling condition again after set to the disabling condition.

If the over current condition occurred when the input voltage value was close to the minimum operating input voltage value. Under this condition, the voltage descends by the parasitic impedance on the power supply side, and it might fall below the detection threshold of the UVLO circuit. In this case, the switch-transistor is turned OFF and because of that the voltage drop of power line's parasitic impedance stops; the latch function is released with the UVLO and it becomes the over current condition again. The switch transistor keeps continual ON and OFF until one of the following is done; increasing the input voltage value; the setting of EN pin is disabling; or reducing the value of load current.

Moreover, the supply-voltage changed by the load-current dramatically changed depends upon the parasitic impedance of the wiring on the load side or the power supply side. Due to this, decreasing the parasitic impedance by the wiring on board is recommended.

The switch transistor of the R5524x001A/001B is turned OFF when the latch-off-function operates under the condition of the load of the constant current as the load device, such as the electronic load and so on, connecting with the V_{OUT} pin of the R5524x001A/001B. Because the load device keeps the constant current, the V_{OUT} pin voltage may become negative potential. If the V_{OUT} pin is exceed the absolute maximum rating may cause the permanent damages to the device, please avoid using in this situation.

The R5524x002A/002B and R5524N004A have the built-in over current protection circuit as the constant current type. It detects as the over-current condition, if the current flows as the ITH defined. Then operating the switch transistor to limit the output current to be the constant current defined by the I_{LIM}.

If the condition of the over-current limit caused by the V_{OUT} pin clamped to the GND were continued the temperature of the ICs would increase drastically. The switch-transistor is turned OFF if the temperature of the ICs becomes over 135°C (Typ.). And after this, the switch-transistor is turned ON again when the temperature of ICs decreased approximately 15°C. The switch-transistor keeps continual ON and OFF until either the switch is turned OFF or the V_{OUT} pin is removed from GND.

PACKAGE INFORMATION

Power Dissipation (SOT-23-5)

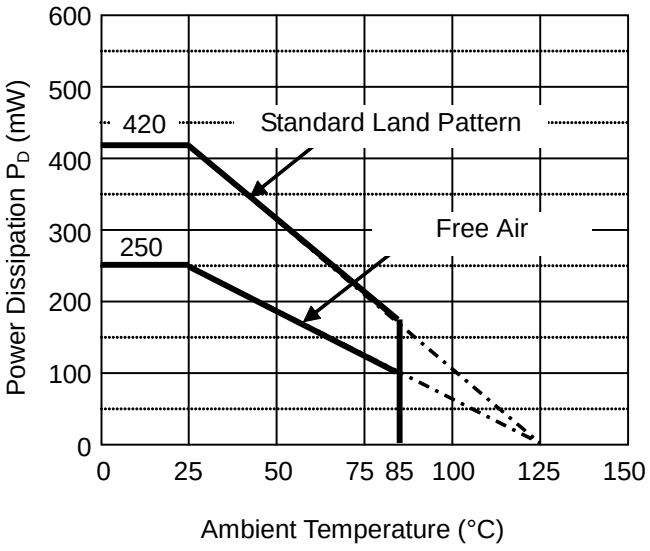
Power Dissipation (P_D) of the package is dependent on PCB material, layout, and environmental conditions. The following conditions are used in this measurement. This data is taken from a SOT-23-6 package data.

Measurement Conditions

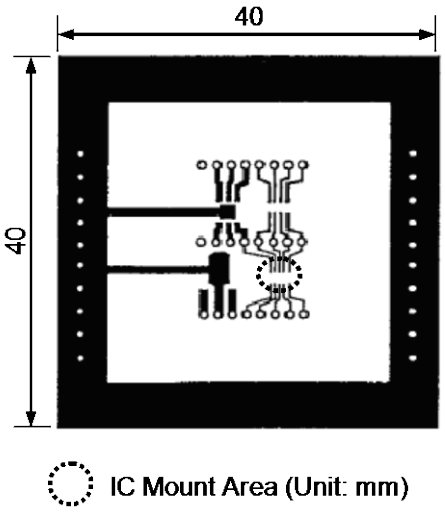
	Standard Land Pattern
Environment	Mounting on Board (Wind Velocity = m/s)
Board Material	Glass Cloth Epoxy Plastic (Double-sided)
Board Dimensions	40 mm × 40 mm × 1.6 mm
Copper Ratio	Top-side: Approx. 50%, Back-side: Approx. 50%
Through-holes	ϕ 0.5 mm × 44 pcs

Measurement Result (Ta = 25°C, Tjmax = 125°C)

	Standard Land Pattern	Free Air
Power Dissipation	420 mW	250 mW
Thermal Resistance	Θja = (125 − 25°C) / 0.42 W = 238°C/W	400°C/W

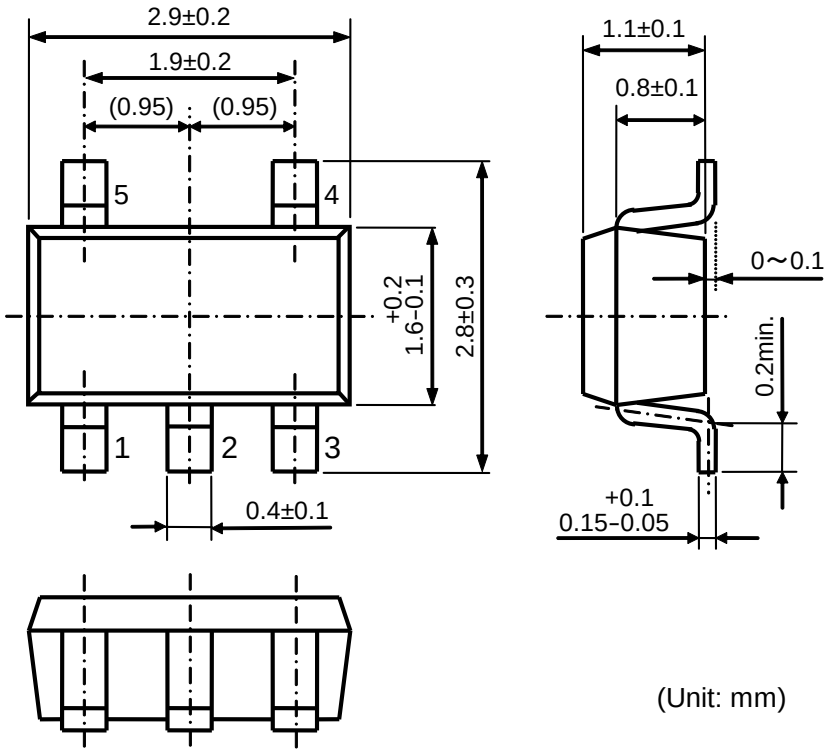


Power Dissipation vs. Ambient Temperature



Measurement Board Pattern

PACKAGE DIMENSIONS (SOT-23-5)



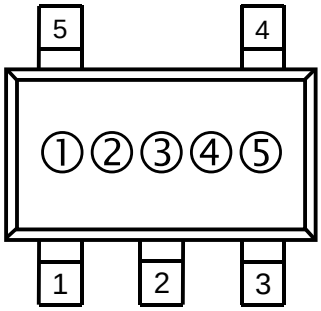
(Unit: mm)

SOT-23-5 Package Dimensions

MARK SPECIFICATION (SOT-23-5)

①②③: Product Code … **Refer to *MARK SPECIFICATION TABLE (SOT-23-5)***

④⑤: Lot Number … Alphanumeric Serial Number



SOT-23-5 Mark Specification

MARK SPECIFICATION TABLE (SOT-23-5)

Mark Specification Table

Product Name	①②③
R5524N001A	M A A
R5524N001B	M A B
R5524N002A	M A C
R5524N002B	M A D
R5524N004A	M A F

POWER DISSIPATION (DFN(PLP)1820-6)

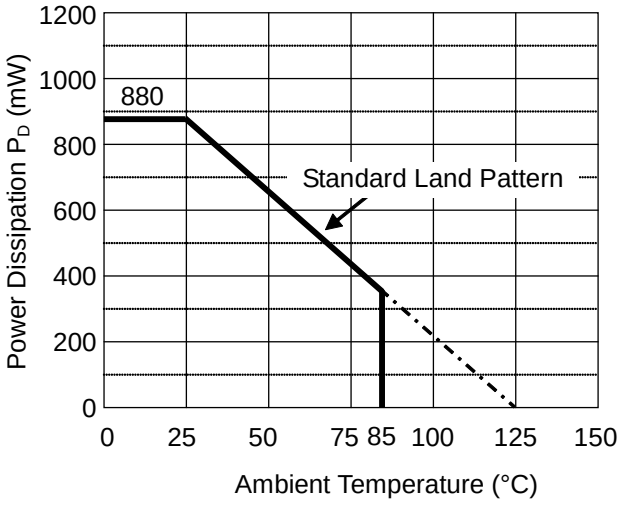
Power Dissipation (P_D) of the package is dependent on PCB material, layout, and environmental conditions. The following conditions are used in this measurement.

Measurement Conditions

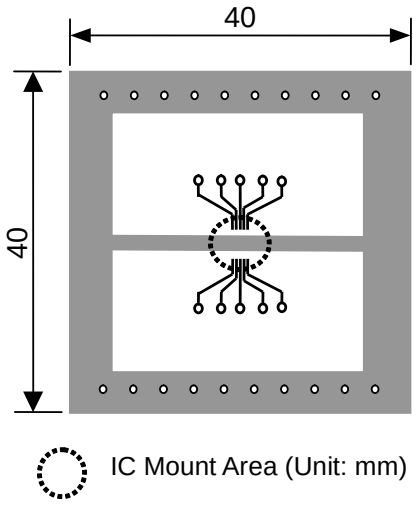
	Standard Land Pattern
Environment	Mounting on Board (Wind Velocity = 0 m/s)
Board Material	Glass Cloth Epoxy Plastic (Double-sided)
Board Dimensions	40 mm × 40 mm × 1.6 mm
Copper Ratio	Top-side: Approx. 50%, Back-side: Approx. 50%
Through-hole	ϕ 0.54 mm × 30 pcs

Measurement Result (Ta = 25°C, Tjmax = 125°C)

	Standard Land Pattern
Power Dissipation	880 mW
Thermal Resistance	Θja = (125 − 25°C) / 0.88 W = 114°C/W

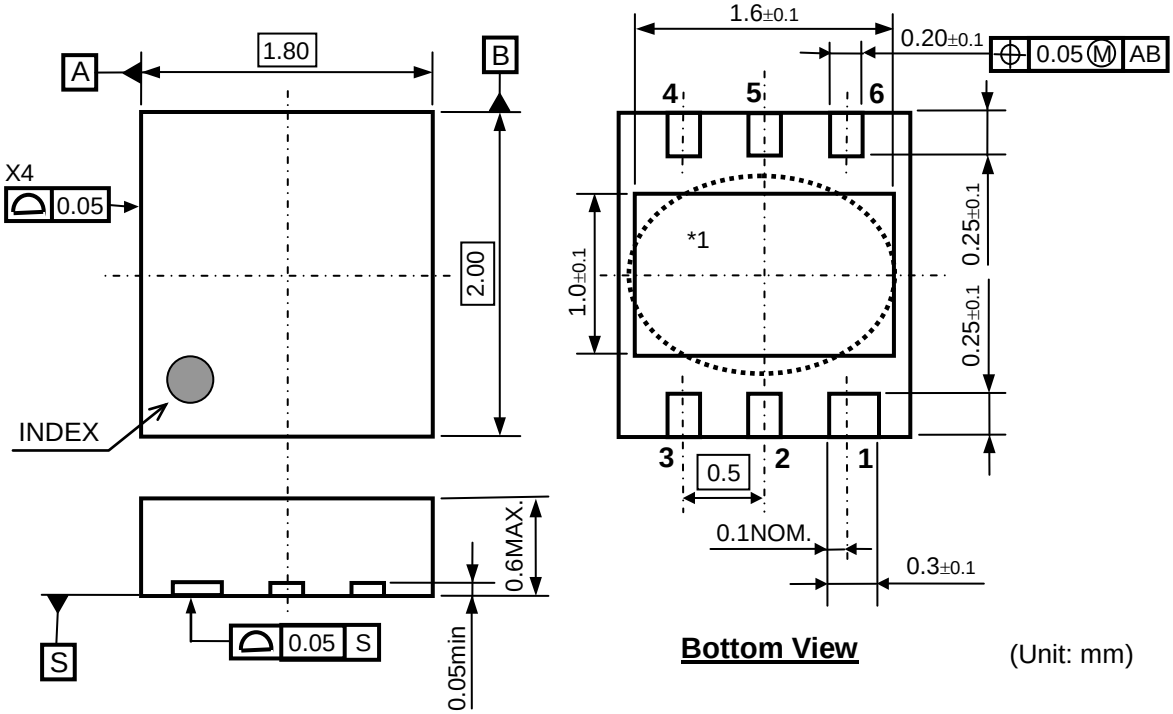


Power Dissipation vs. Ambient Temperature



Measurement Board Pattern

PACKAGE DIMENSIONS (DFN(PLP)1820-6)



(Unit: mm)

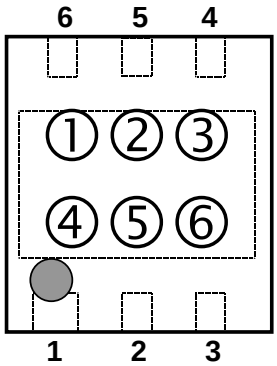
*1 The tab on the bottom of the package enhances thermal performance and is electrically connected to GND (substrate level). It is recommended that the tab be connected to the ground plane on the board, or otherwise be left floating.

DFN(PLP)1820-6 Package Dimensions

MARK SPECIFICATION (DFN(PLP)1820-6)

①②③④: Product Code …**Refer to *MARK SPECIFICATION TABLE (DFN(PLP)1820-6***

⑤⑥: Lot Number …Alphanumeric Serial Number



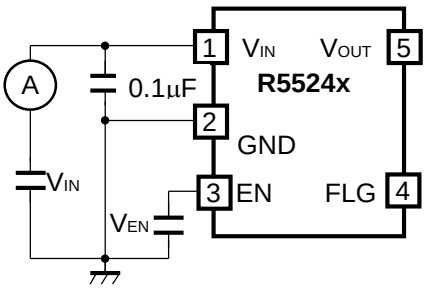
DFN(PLP)1820-6 Mark Specification

MARK SPECIFICATION TABLE (DFN(PLP)1820-6)

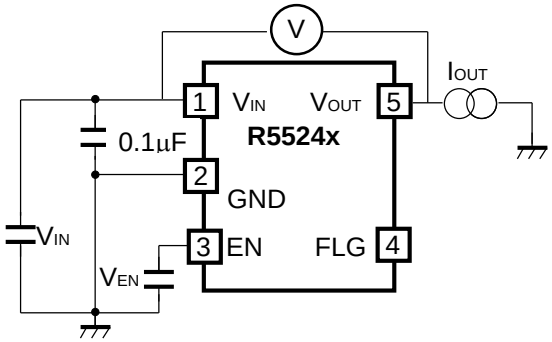
Mark Specification Table

Product Name	①②③④
R5524K001A	E J 0 0
R5524K001B	E J 0 1
R5524K002A	E J 0 2
R5524K002B	E J 0 3

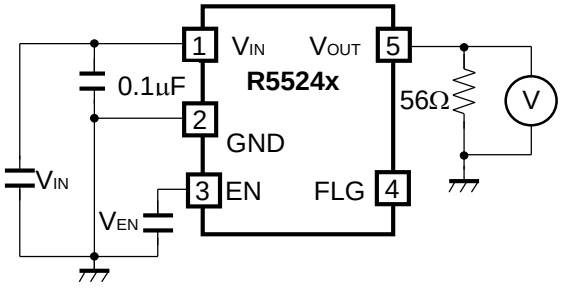
TEST CIRCUITS



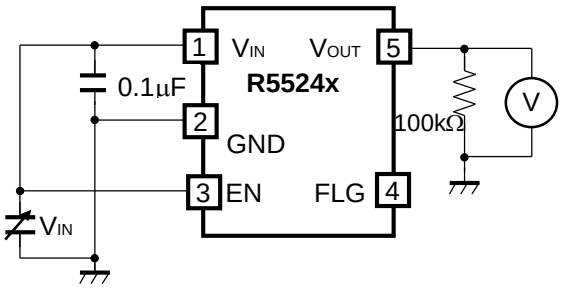
Supply Current Test Circuit



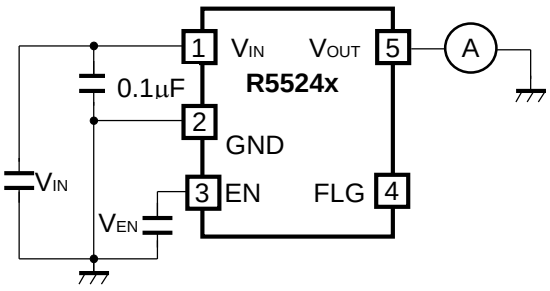
Switch ON Resistance Test Circuit



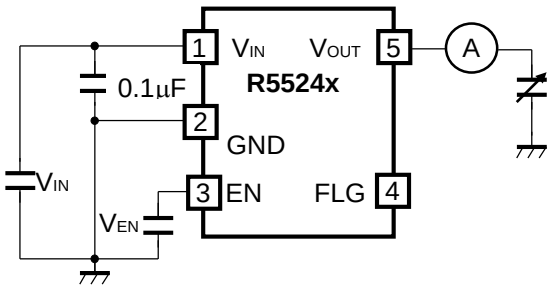
Output ON Time/Output OFF Time Test Circuit



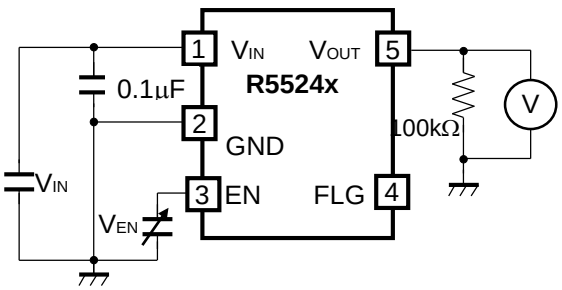
UVLO Released Voltage Test Circuit



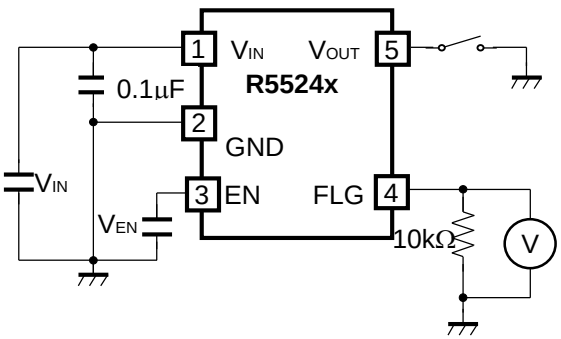
Over current Limit Test Circuit



Current Limit Threshold Test Circuit



Enable Input Voltage Test Circuit

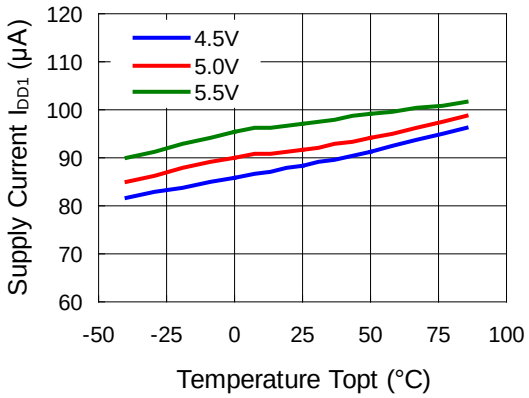


Flag Output Delay Time Test Circuit

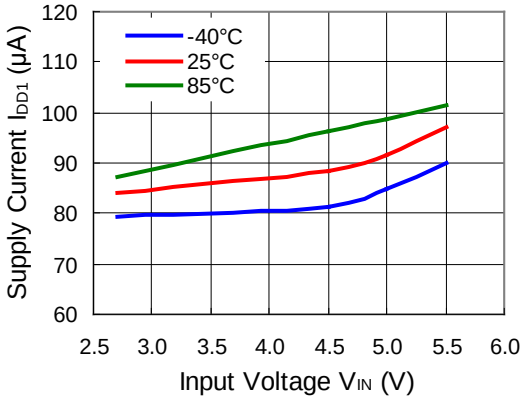
TYPICAL CHARACTERISTICS

Note: Typical Characteristics are intended to be used as reference data; they are not guaranteed.

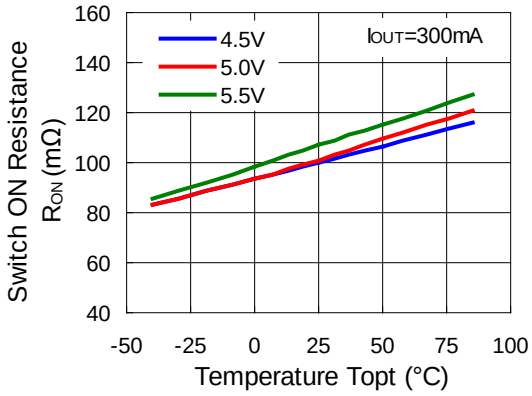
1) Supply Current vs. Temperature



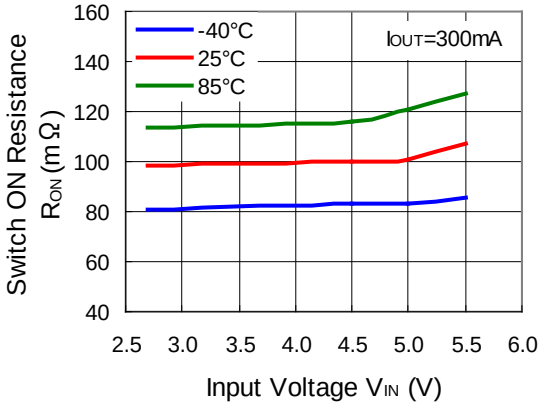
2) Supply Current vs. Input Voltage



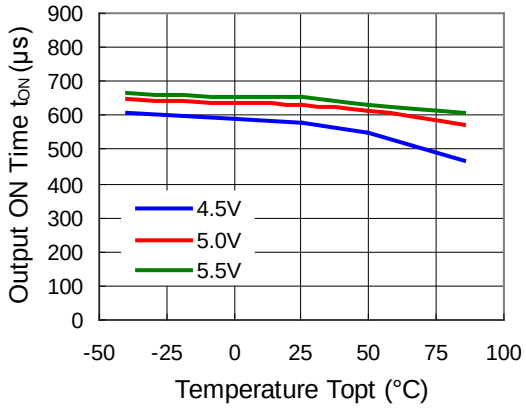
3) Switch ON Resistance vs. Temperature



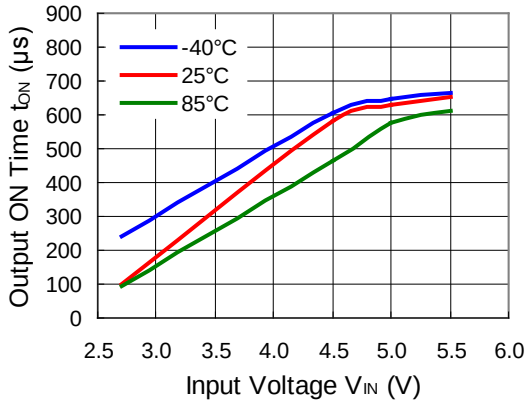
4) Switch ON Resistance vs. Input Voltage



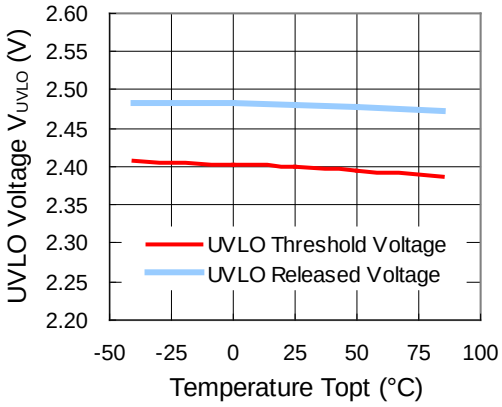
5) Output ON Time vs. Temperature (R_L = 56 Ω)



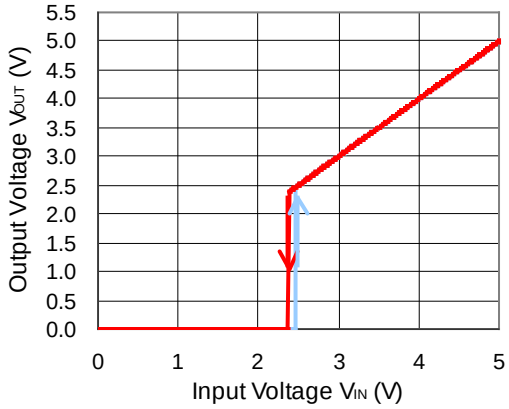
6) Output ON Time vs. Input Voltage (R_L = 56 Ω)



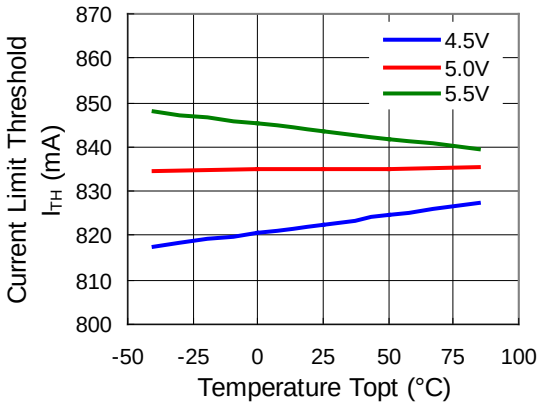
7) UVLO Voltage vs. Temperature



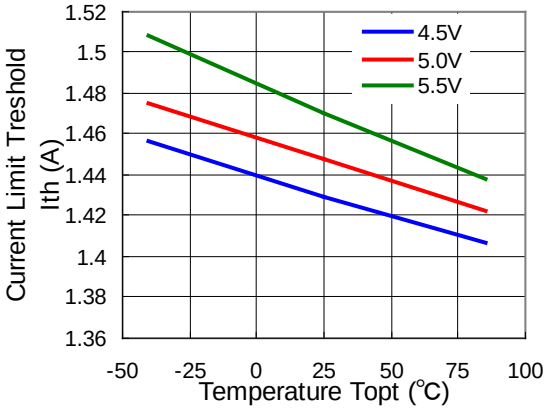
8) Output Voltage vs. Input Voltage



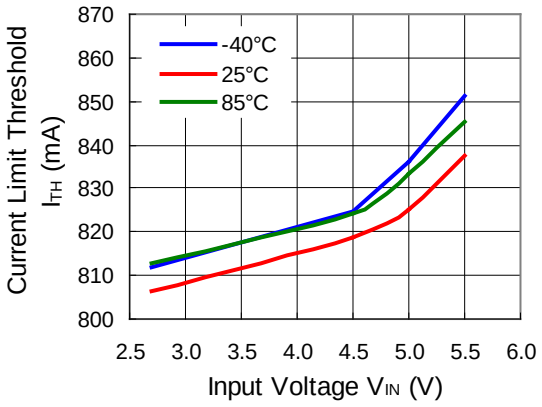
9) Current Limit Threshold vs. Temperature (001x/ 002x)



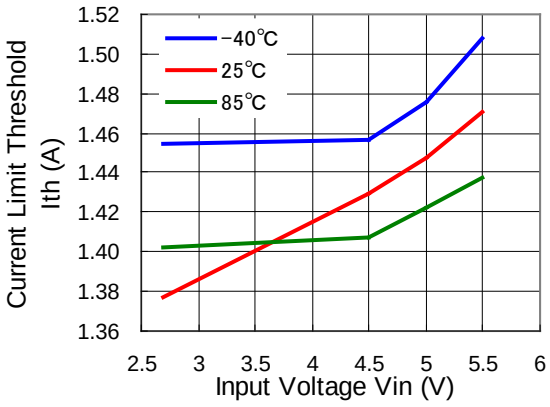
10) Current Limit Threshold vs. Temperature (004A)



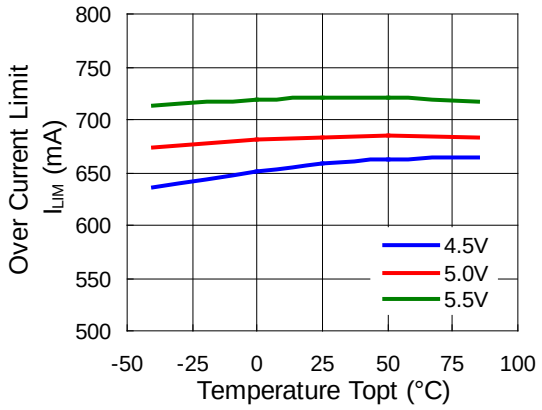
11) Current Limit Threshold vs. Input Voltage (001x/ 002x)



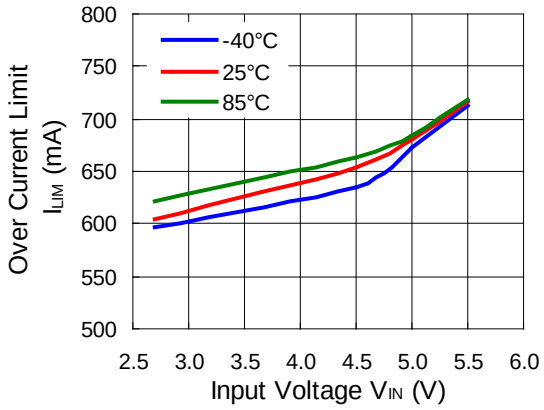
12) Current Limit Threshold vs. Input Voltage (004A)



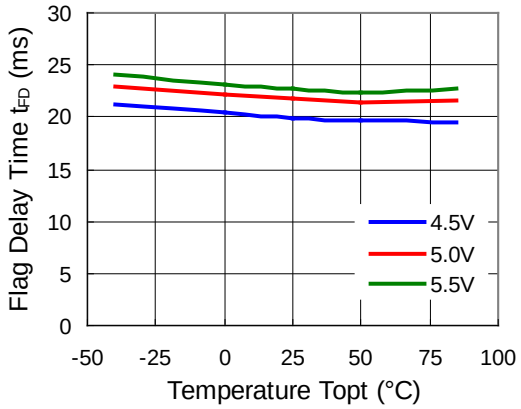
13) Overcurrent Limit vs. Temperature



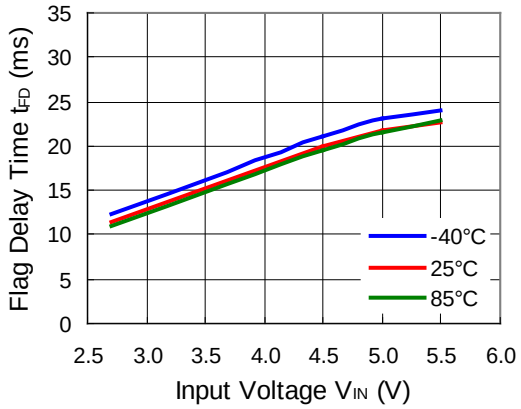
14) Overcurrent Limit vs. Input Voltage



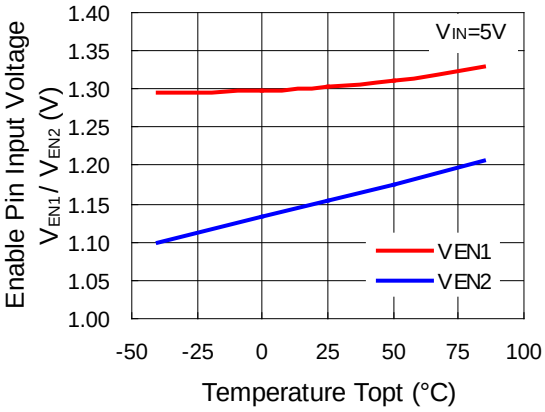
15) Flag Delay Time vs. Temperature



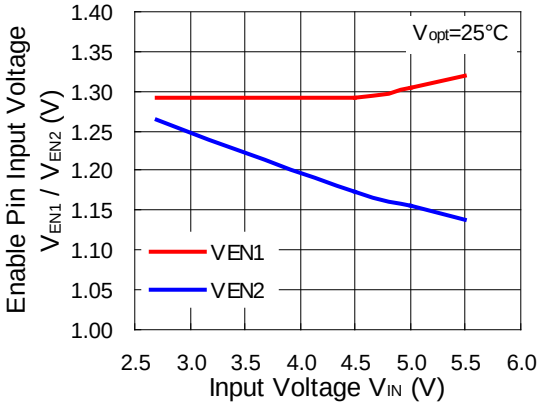
16) Flag Delay Time vs. Input Voltage



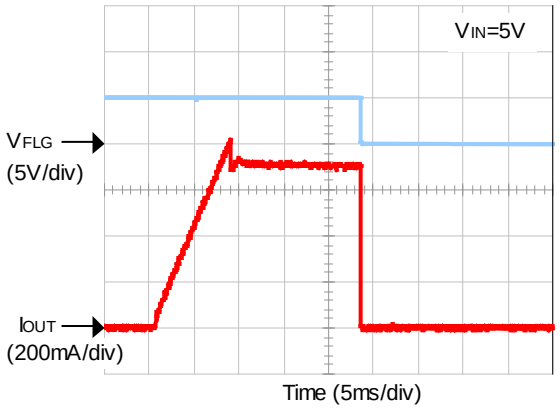
17) Enable Input Voltage vs. Temperature



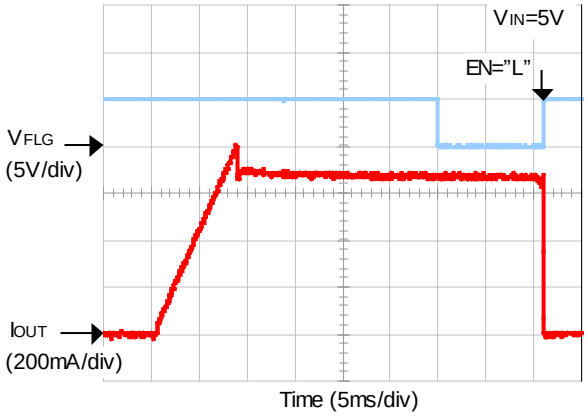
18) Enable Input Voltage vs. Input Voltage



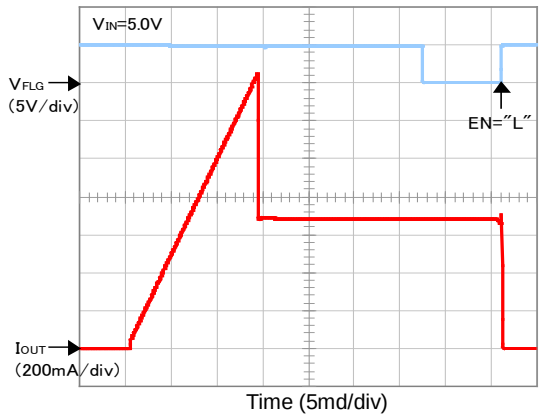
19) Overcurrent Response with Ramped Load (R5524x001x)



20) Overcurrent Response with Ramped Load (R5524x002x)

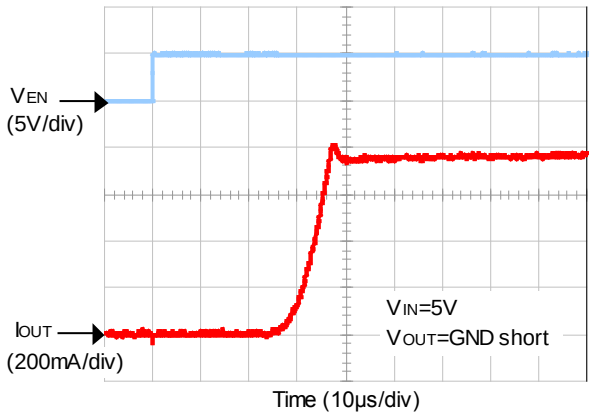


21) Overcurrent Response with Ramped Load (R5524x004A)

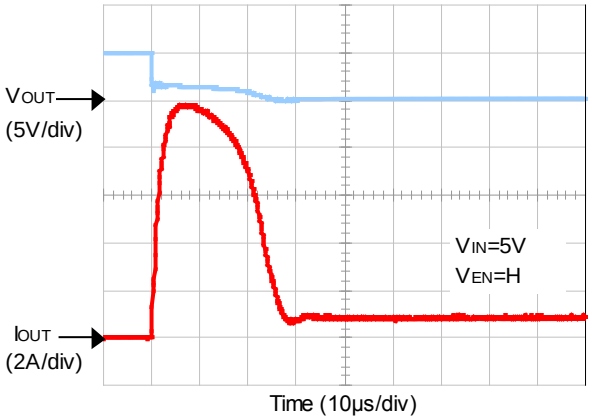


22) Overcurrent Limit Transient Response

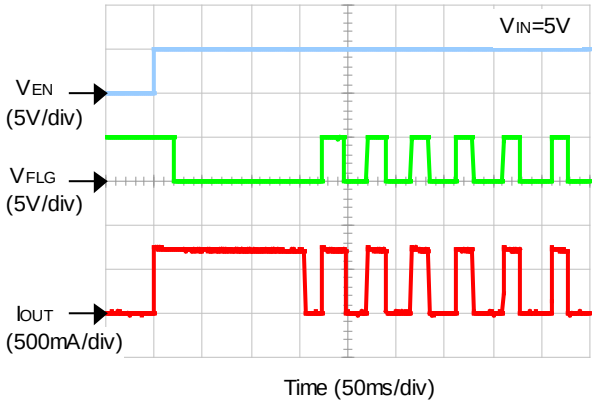
(Output short during enable "H")



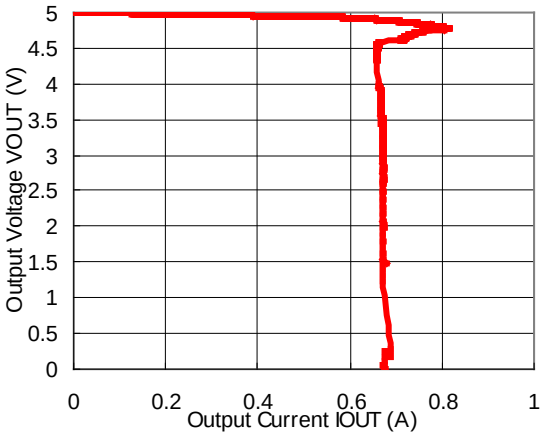
(Enable "H" during Output Short)



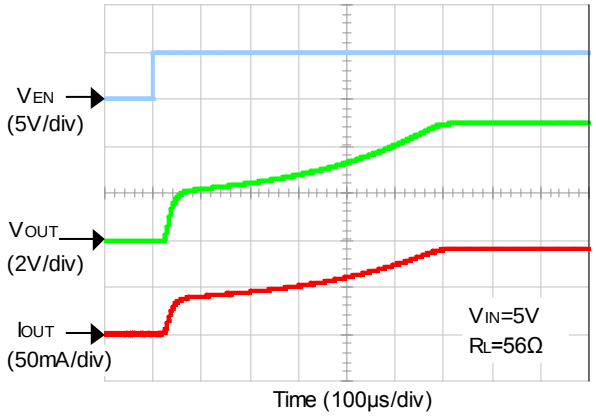
23) Thermal Shutdown Operation



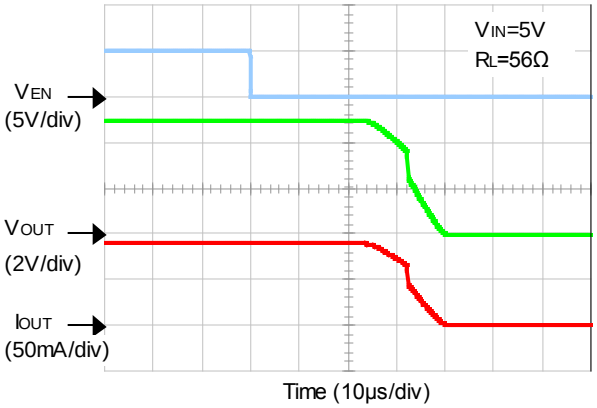
24) Output Voltage vs. Output Current



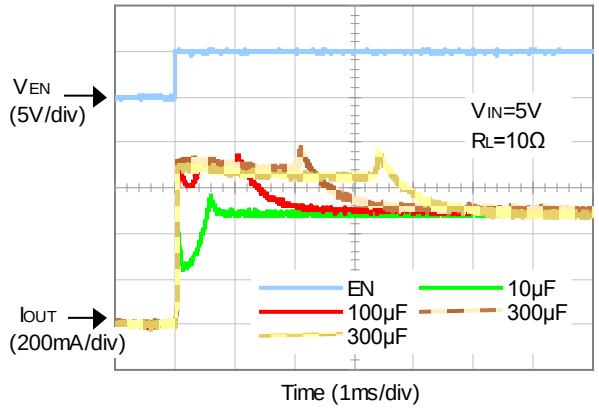
25) Output ON Time Response



26) Output OFF Time Response



27) Inrush current Characteristic



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Sales & Support Offices

RICOH ELECTRONIC DEVICES CO., LTD.
Higashi-Shinagawa Office (International Sales)
3-32-3, Higashi-Shinagawa, Shinagawa-ku, Tokyo 140-8655, Japan
Phone: +81-3-5479-2857 Fax: +81-3-5479-0502

RICOH EUROPE (NETHERLANDS) B.V.
Semiconductor Support Centre
Prof. W.H. Keesomlaan 1, 1183 DJ Amstelveen, The Netherlands
Phone: +31-20-5474-309

RICOH INTERNATIONAL B.V. - German Branch
Semiconductor Sales and Support Centre
Oberrather Strasse 6, 40472 Düsseldorf, Germany
Phone: +49-211-6546-0

RICOH ELECTRONIC DEVICES KOREA CO., LTD.
3F, Haesung Bldg, 504, Teheran-ro, Gangnam-gu, Seoul, 135-725, Korea
Phone: +82-2-2135-5700 Fax: +82-2-2051-5713

RICOH ELECTRONIC DEVICES SHANGHAI CO., LTD.
Room 403, No.2 Building, No.690 Bibo Road, Pu Dong New District, Shanghai 201203, People's Republic of China
Phone: +86-21-5027-3200 Fax: +86-21-5027-3299

RICOH ELECTRONIC DEVICES CO., LTD.
Taipei office
Room 109, 10F-1, No.51, Hengyang Rd., Taipei City, Taiwan (R.O.C.)
Phone: +886-2-2313-1621/1622 Fax: +886-2-2313-1623